LA-UR-18-28870
Approved for public release; distribution is unlimited.

Title: Digital Control System Performance for the LANSCE Accelerator System

Author(s): Kwon, Sung Il

Intended for: Invitation Talk, Institute of the Basic Science, Republic of Korea

Issued: 2018-09-19

Digital Control System Performance for the LANSCE Accelerator System

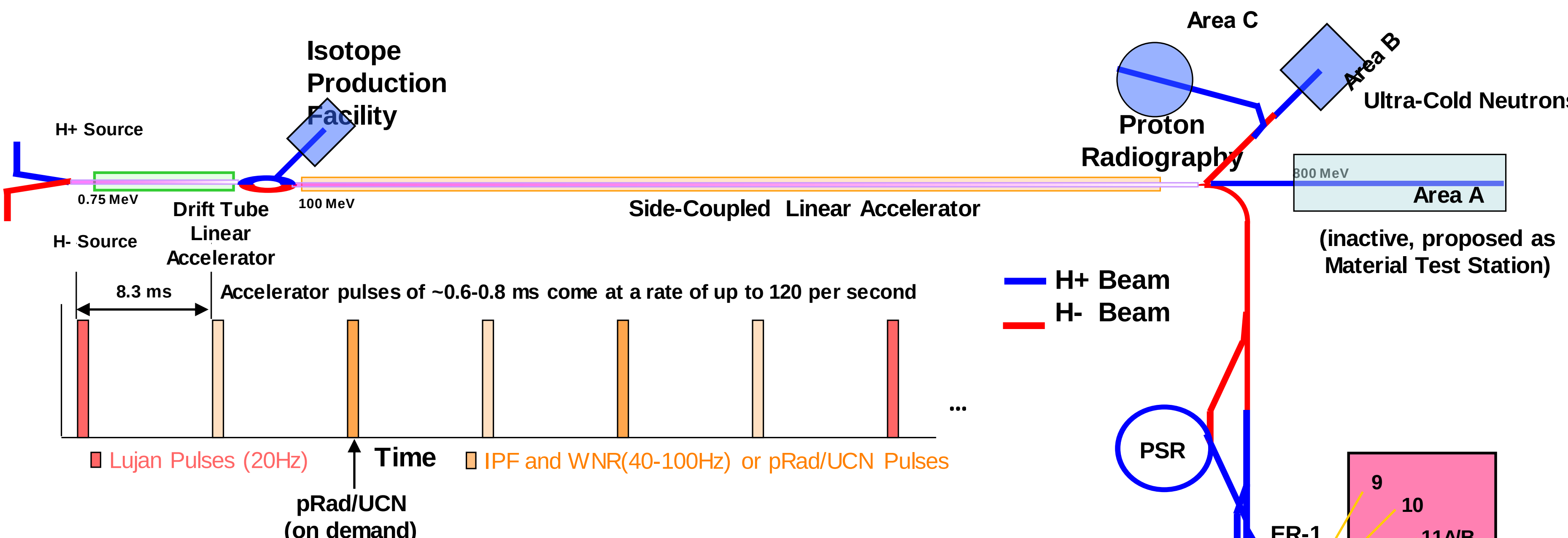
Sungil Kwon

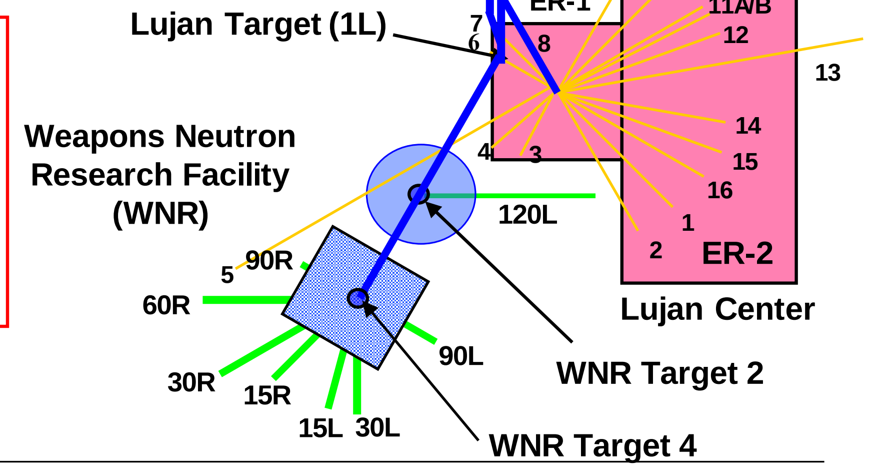
Accelerator Operation and Technology Division

Los Alamos National Laboratory

The LANSCE accelerator provides uniquely flexible time-structured beams from 100 to 800 MeV that serve >20 active experimental stations

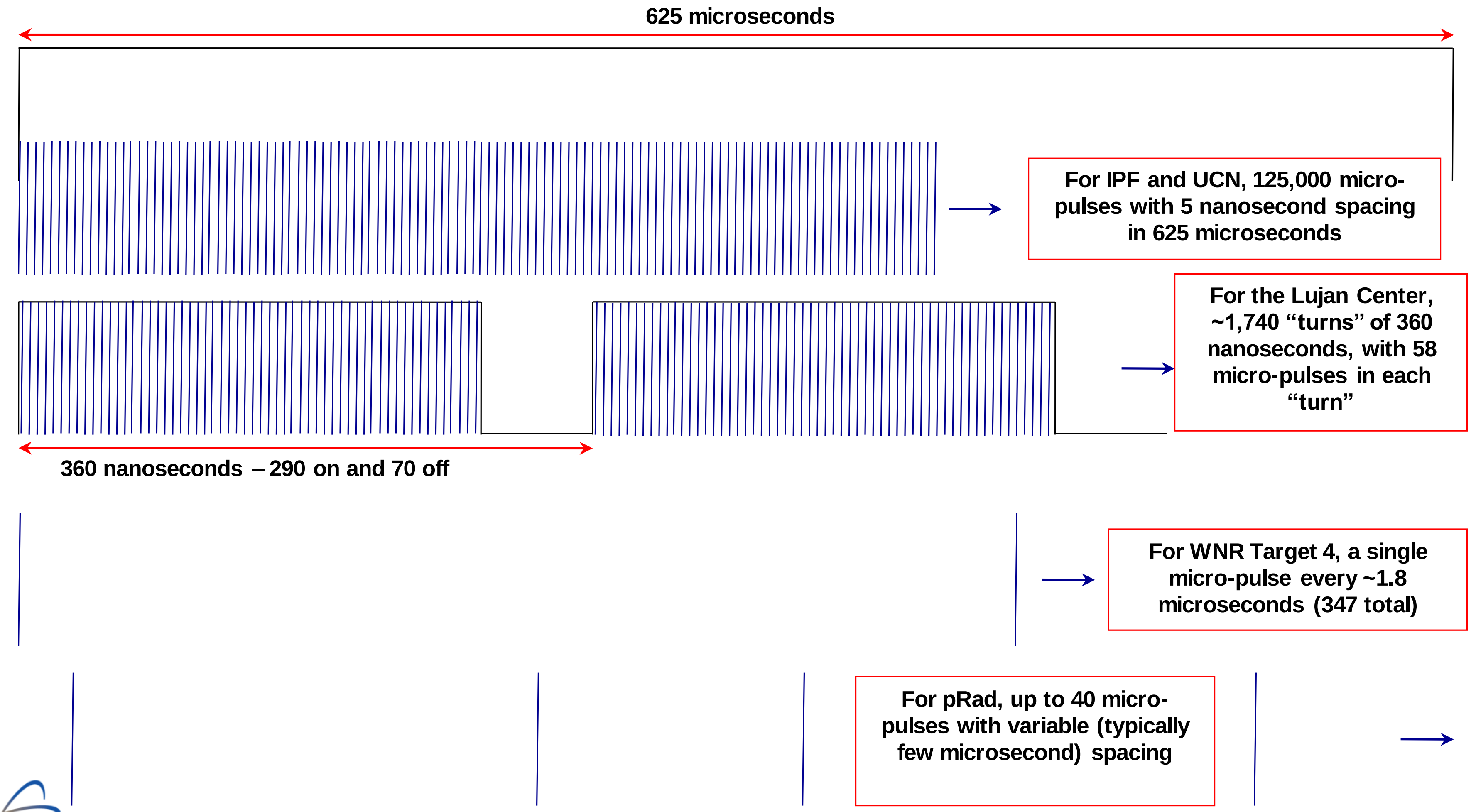
LANSCE provides uniquely time-structured pulsed beams of varying power levels "simultaneously" to five different experimental areas





LANSCE delivers:
Up to 120 beam cycles per second each of length of 625-825 microseconds, with single pulse capability of 1225 microseconds
Within each cycle 1 nanosecond beam micro-pulses with a minimum separation of 5 nanoseconds
20 Hz are dedicated for the Lujan Center
40-100 Hz are available for multiplexed use by pRad, WNR, IPF, UCN
IPF (H+) and WNR (H-) share machine cycles
pRad and UCN "steal" on-demand machine cycles from WNR

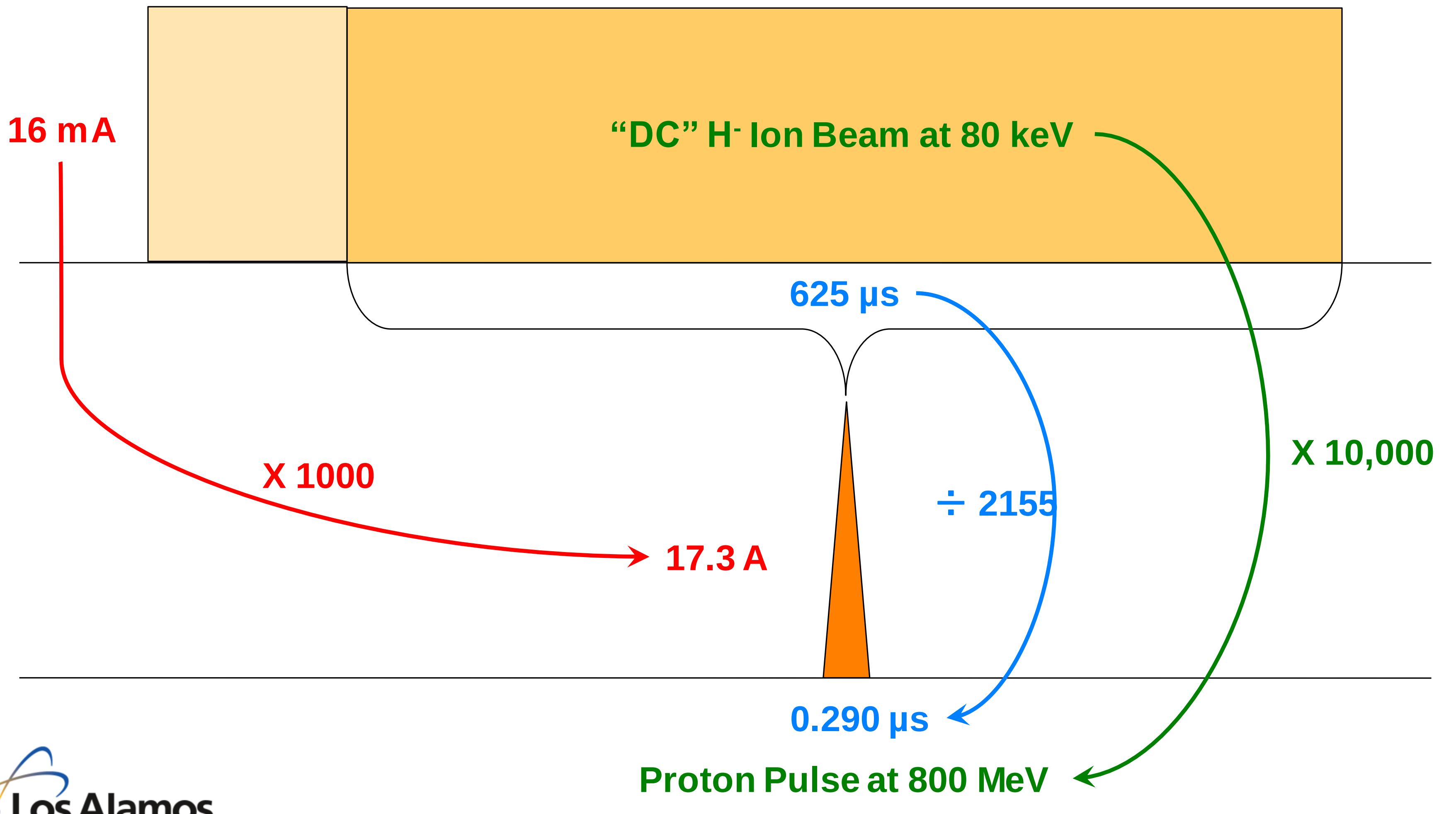
The time structure of the five beams have significant differences



Los Alamos NATIONAL LABORATORY EST. 1943

NNSA

From birth in the ion source to impact on the target to make neutrons, each of the 20 Hz proton pulses that strike the Lujan target undergoes a complex evolution



This presentation discusses the basic hardware and associated physics needed to increase the energy, impose the proper temporal structure and compress the charge to make the desired neutron flux from the Lujan target

- Energy Increase is obtained using three different accelerating structures:
  - Electrostatic lens accelerator (0 to 750 keV)
  - Radio-frequency Drift Tube linear accelerator
  - Radio-frequency Side-Coupled Cavity linear accelerator
- Temporal Structure is imposed by:
  - Choppers
  - Radio-Frequency bunchers
- Peak Current Increase is obtained through the:
  - Proton Storage Ring

The LANSCE accelerator generates beams of protons or negative hydrogen ions for neutron production or other experimental applications

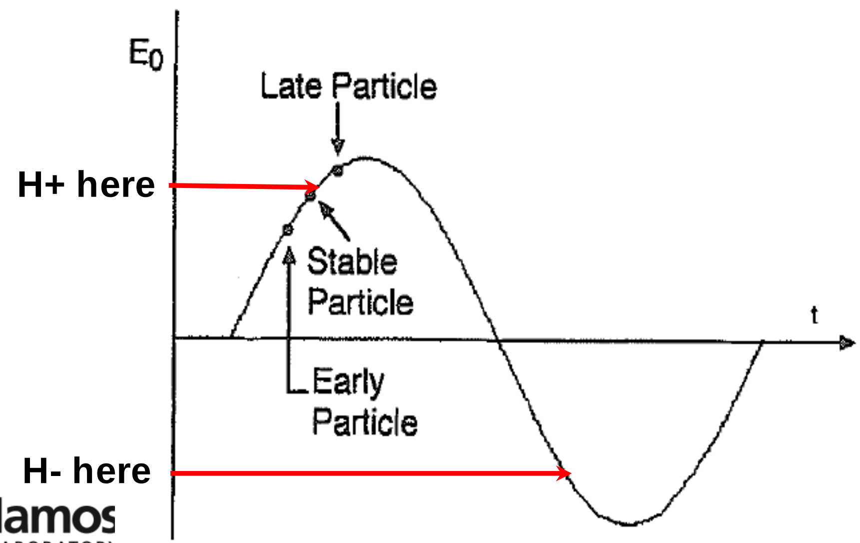
- Very strong electric fields applied to charged particles result in a force that accelerates the particles and increases their kinetic energy
- The LANSCE accelerator uses two different methods to generate the electric fields that impart the energy
  - Electrostatic Cockcroft-Walton Generators (DC High Voltage)
  - Pulsed Radio-frequency (RF) driven resonant cavities
- LANSCE employs two distinct resonant cavity structures to efficiently accelerate the beams from 0.750 MeV (4% the speed of light) to 800 MeV (84% the speed of light)
  - The Drift Tube Linear accelerator (DTL) from 0.750 MeV to 100 MeV
  - The Side-Coupled Cavity Linear accelerator from 100 MeV to 800 MeV
- Each of the five experimental areas described previously uses a beam with a unique temporal structure

A number of key systems enable the LANSCE accelerating structures to perform the core functions of accelerating, tailoring and compressing the beams

- Safety systems separate workers from very high sources of ionizing radiation
- High- and Low-power Radio Frequency systems provide the stable and properly timed electromagnetic fields necessary to accelerate the beams
- Electromagnets are needed to confine the beam particles in the vacuum envelope by focusing and to direct them to the appropriate location by bending and steering:
  - Maintain the desired beam parameters
  - Manage beam losses at levels suitable for hands-on maintenance
- Water systems provide resonance control of and extract waste heat from the resonant accelerating structures, and cool other equipment such as magnets
- Vacuum systems provide the the high vacuum environment to minimize particle collisions with air molecules, and stripping of H^- to H^0/H^+
- Diagnostic devices measure beam profiles, position and emittance
- Loss monitors enable fast (non-human-intervention) beam shut down in the event of equipment set point drifts
- Controls networks, the timing system, and controls hardware and software permit synchronization, adjustment and monitoring of equipment together with data archiving functions and also provide tools to conduct beam tune-up and analyze beam performance

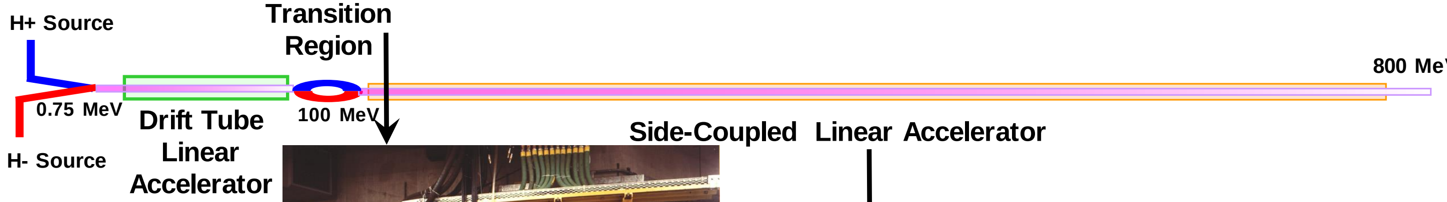
Before we look at accelerating structures we need to understand how RF acceleration works

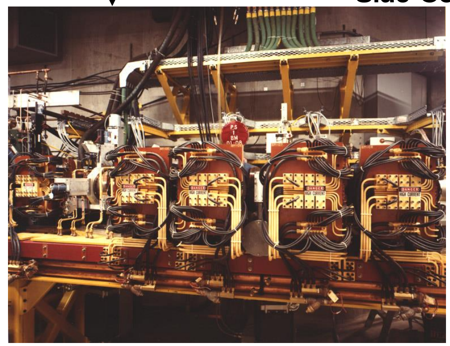
- **Proton linacs such as LANSCE operate on the principle of phase-stable acceleration using standing-wave structures to accommodate the low phase velocity of the heavy particles**
- **Every beam has a momentum distribution – faster particles will arrive earlier than and slower particles later than the ideal, or synchronous, particle**
- **The point of phase stability is typically about 28 degrees before the voltage maximum**

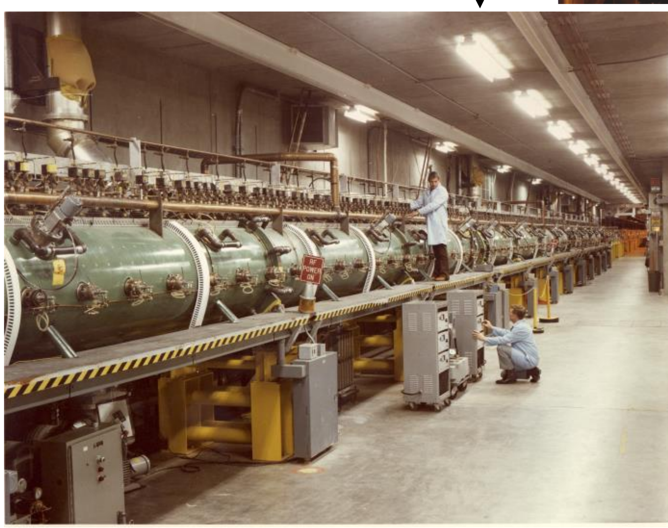


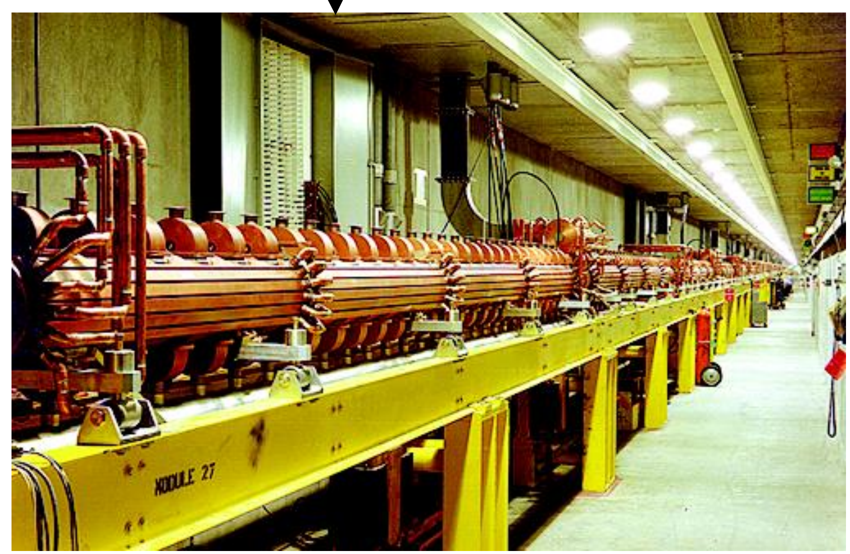
- **Early particles have an energy higher than the synchronous particle, and see a lower field, and hence gain less energy**
- **Late particles have an energy lower than the synchronous particle, and see a higher field, and hence gain more energy**
- **Particles oscillate in a "bucket" around the synchronous particle**

Now that we've covered the basics of beams and focusing, let's take a closer look at the three structures that accelerate the LANSCE beams, together with the LEBT and Transition Region

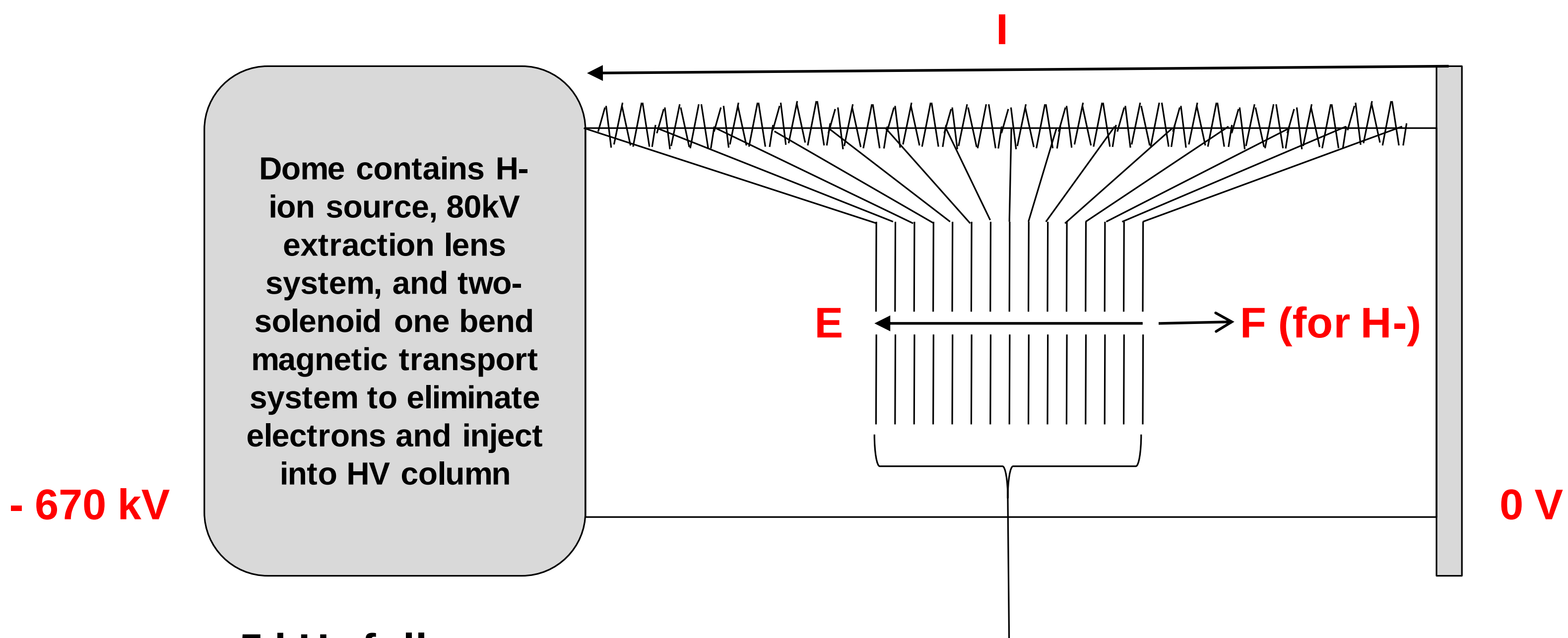








Electrostatic acceleration is straightforward and efficient at low energies (up to a few 10s of MeV) and represented state-of-the-art technology at the time of construction (~1970) – we wouldn't choose to do this today



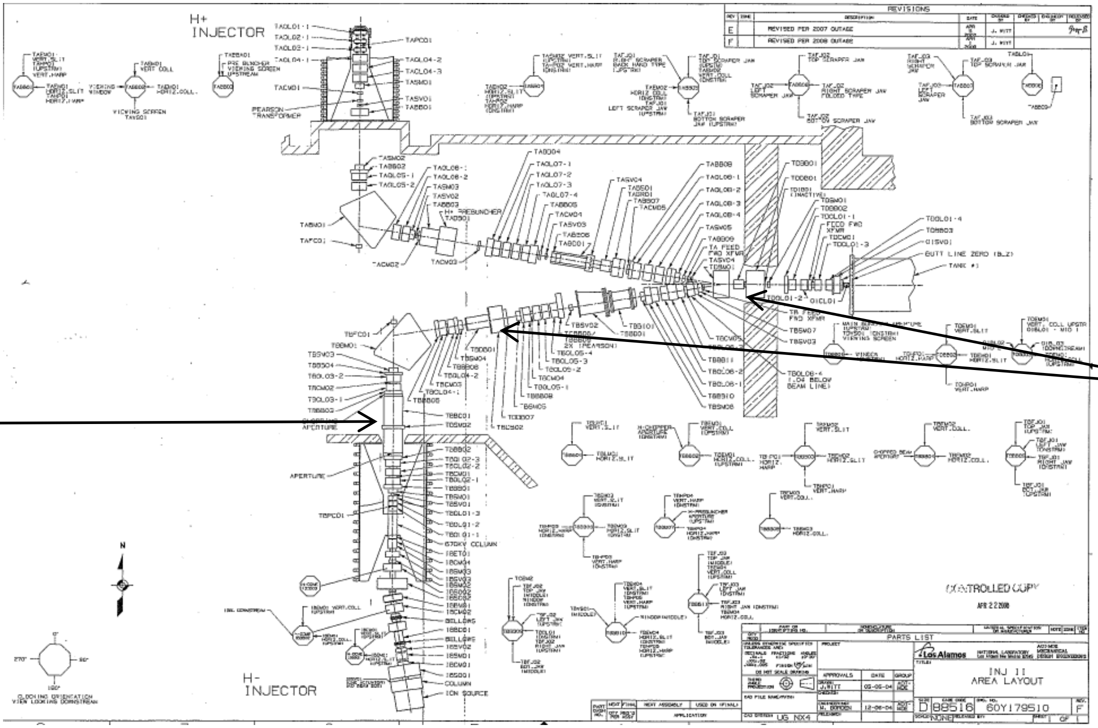
5 kHz full-wave voltage rectifier/multiplier provides 670 +/- 0.1 kV with a low amplitude 10 kHz ripple

Resistive Divider Gap Voltage (14 gaps) is ~48kV

Output of this arrangement is a mono-energetic, continuous 750 keV beam pulse of length 785 μs for each source pulse, up to 120 Hz

The Low Energy Beam Transport (LEBT) gets the beam from the injector to the DTL and also imposes the required temporal structure for each beam

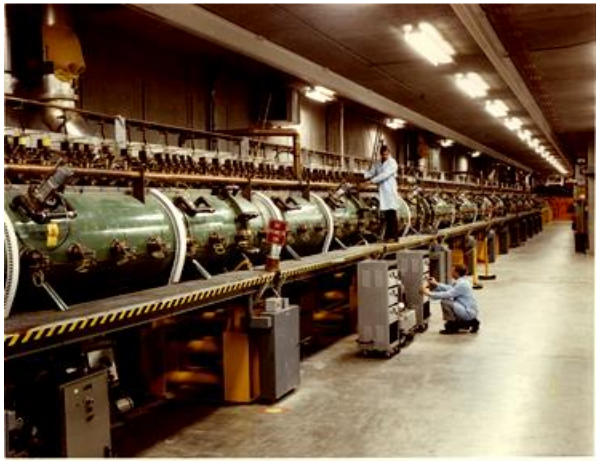
- **Here we “chop” the beam in a traveling-wave helical electric chopper to impose the periodicity required by the Proton Storage Ring (360 ns slices, 250-290 ns beam on followed by a gap of 110-70 ns)**
- **We also impose the 201.25MHz radio-frequency structure on the beam by using two separated sinusoidal voltage bunching cavities**
- **The LEBT also prepares the transverse emittance for matching into the DTL**
- **We also control injection depending on beam permissive conditions**

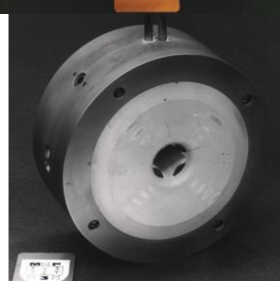


Chopper

201.25MHz Bunchers

The Drift Tube Linear accelerator is an efficient accelerating structure up to about 100 MeV





Details of a drift tube, embedded magnet coil, and and assembled magnet

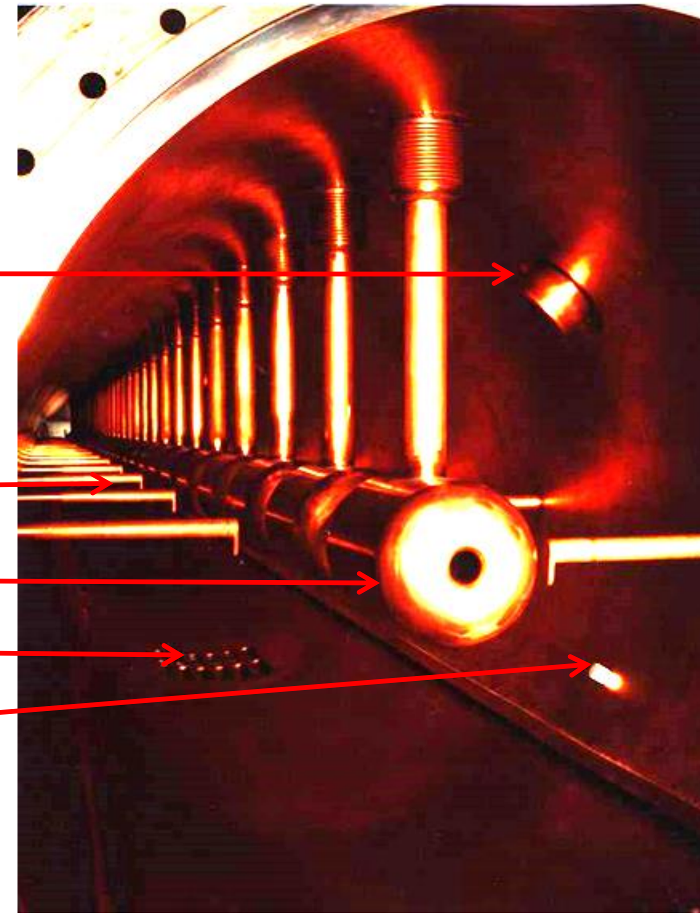
Tuning Slug

Post Coupler

Drift Tube

Vacuum Grate

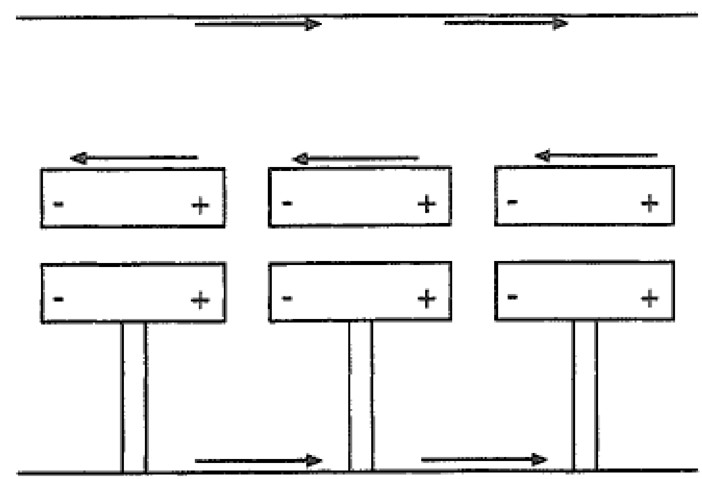
Field Probe

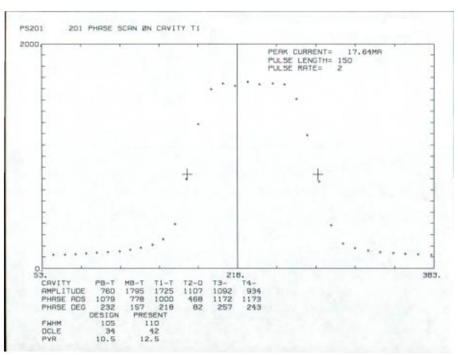


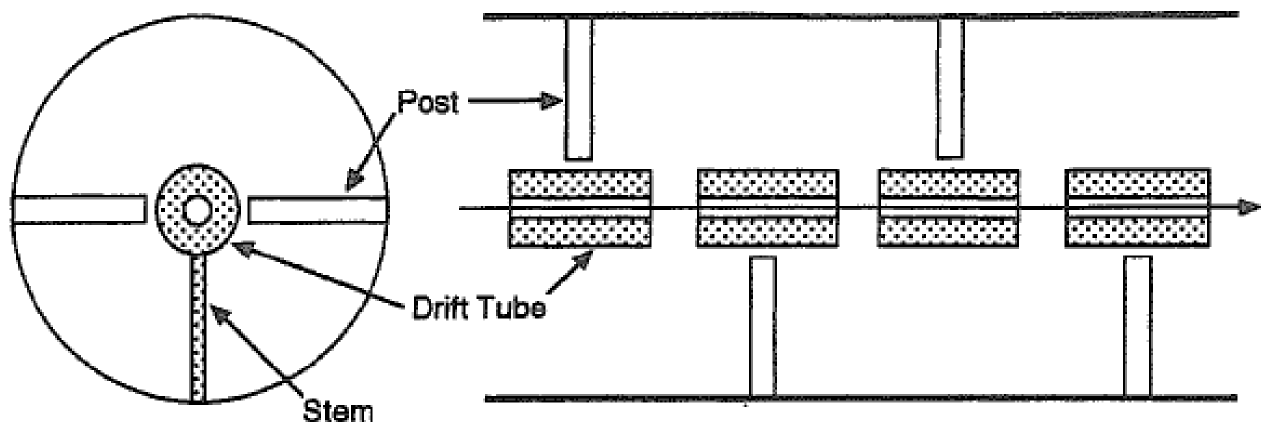
Los Alamos NATIONAL LABORATORY EST. 1943

In the DTL the axial electric fields that provide acceleration oscillate between the ends of the drift tubes in the tuned resonant accelerator cavity

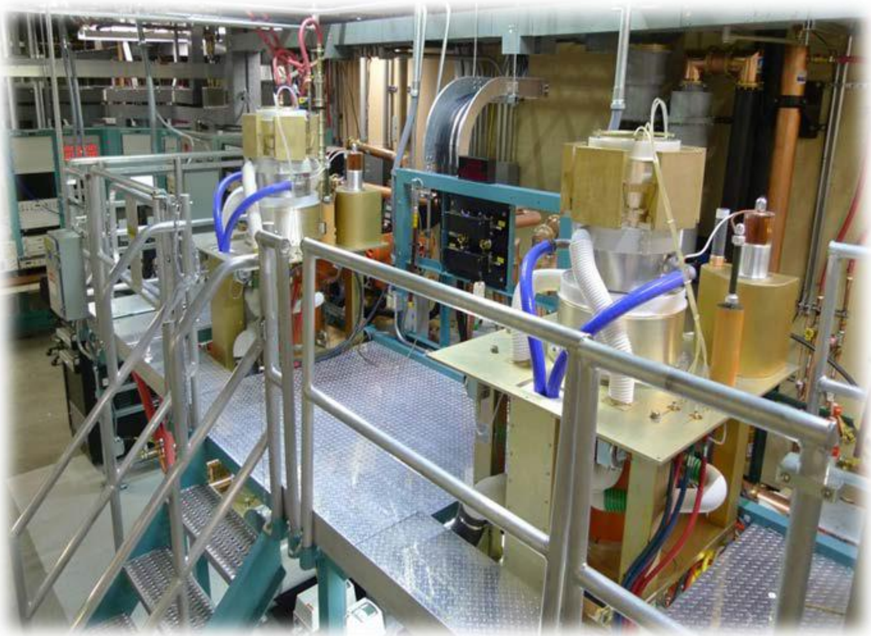
- **The tank is designed to resonate at 201.25 MHz in cylindrical geometry – resonance is controlled by physical size (temperature) and adjusted with the automated tuning slugs**
- **Currents flow to set up the cylindrical magnetic and axial electric fields**
- **The post couplers stabilize the resonant mode, suppress parasitic modes, and improve the propagation time during cavity fill**







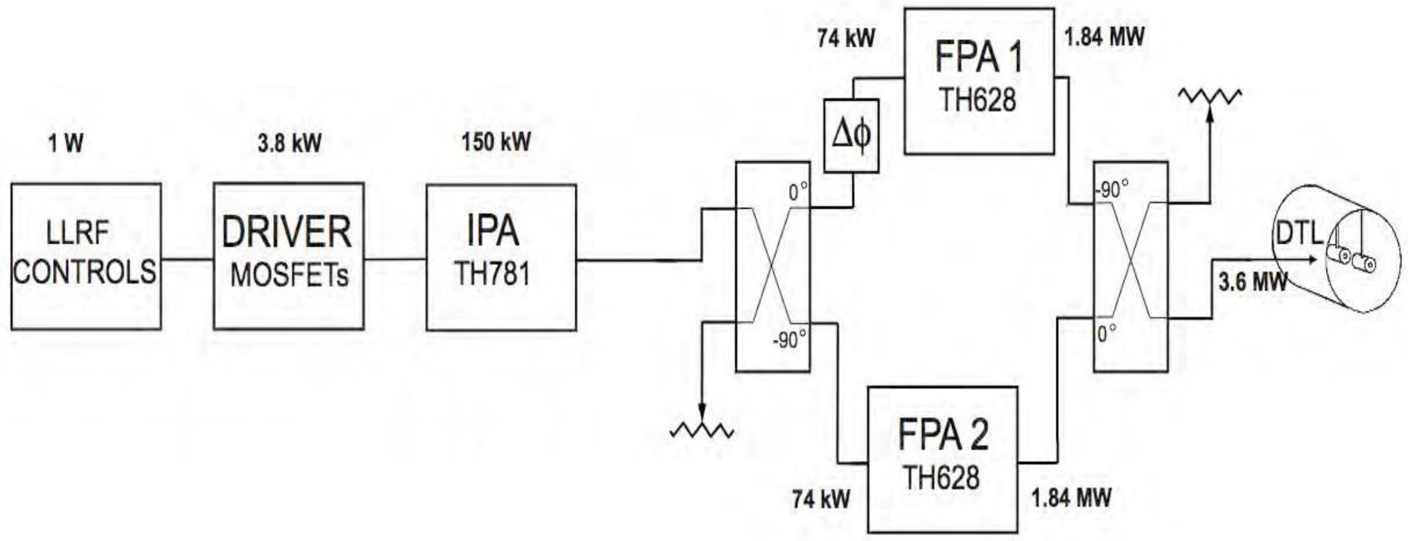
The 201MHz Diacrode, TH628 Thomson(Tales) Diacrode



The 201MHz Diacrode, TH628 Thomson(Tales) Diacrode

- With 3.6 MW and 12% DF planned, we would be operating above the screen grid rating of a single TH628
- 2010 ES&H requirements at Thales forced change in pyrolytic graphite treatment that used silane/borane gas for doping to reduce RF loss; this required further derating of new tube
  - Combining two amplifiers at DTL2, 3 and 4 solved both
- Each TH628 will be operating at 150 kW anode dissipation or 19% of rating, instead of 90% as with the 7835 triode
- Cathode emission requirement reduced due to larger emission area (800 versus 300 cm^2) and lower peak current
  - 3 amps/cm^2 in 7835 and 1 amp/cm^2 in TH628 = significant lifetime improvement predicted, can reduce filament temperature

DTL RF System

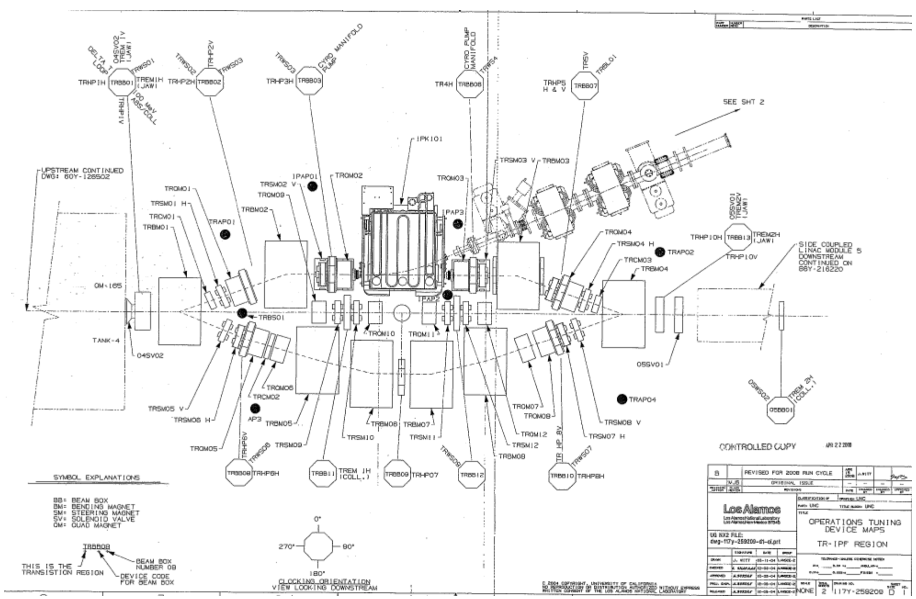


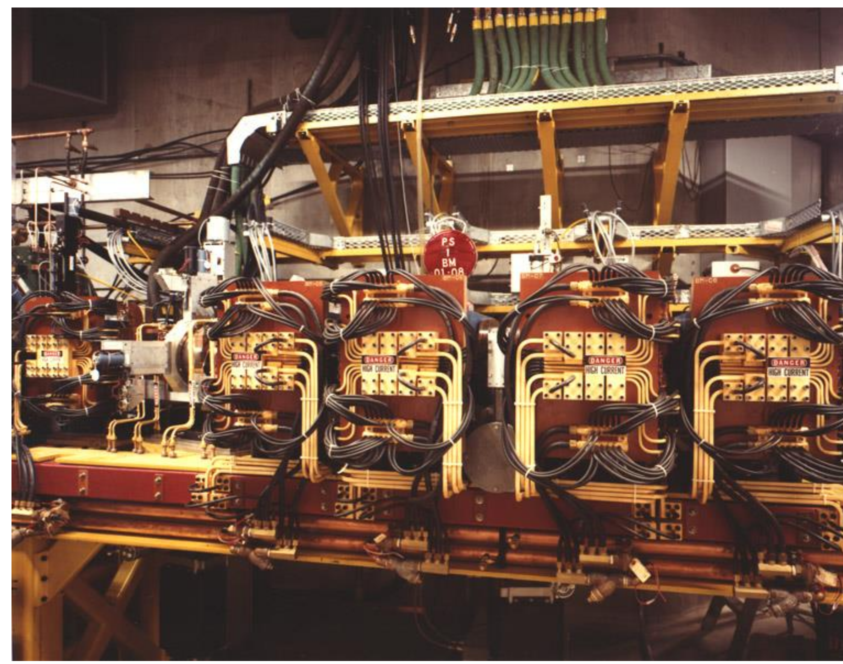
Capacitive Output Coupler

- Copper Bellows
- l/4 Stub for Mechanism
- Easily Removable
- Adjustable Under Power
- Second harmonic suppression

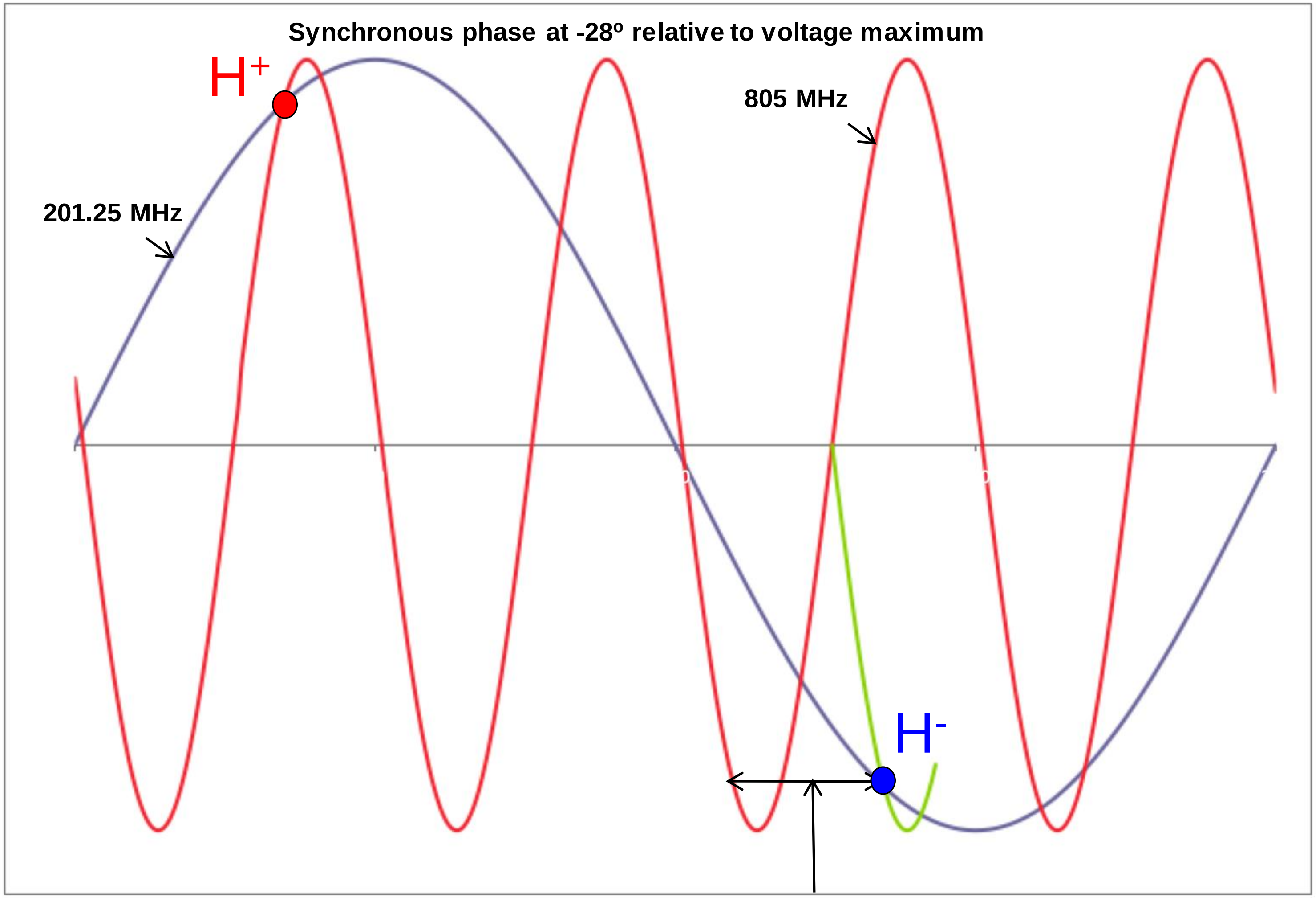
The Transition Region (TR) is needed to perform the longitudinal match between the DTL and CCL for simultaneous transport of H+ and H- beams

- **The TR allows physical separation of H+ and H- beams so that the phase of the H- can be independently adjusted by changing its path length**
- **This allows the phase stable points for each beam to be properly placed on the corresponding phase of the 805 MHz RF in the CCL**
- **The TR also provides the transverse matching from the DTL FODO lattice into the CCL FDO lattice**





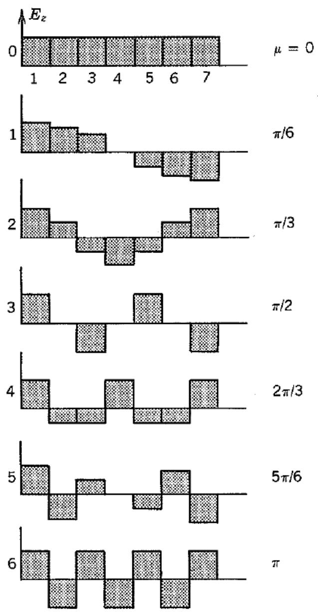
The transition region effectively "delays" the H- beam so that it arrives at the appropriate synchronous phase for acceleration

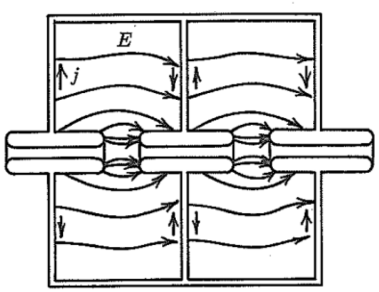


Phase delay introduced by the TR to put H- beam at the phase stable point on the 805 MHz fields

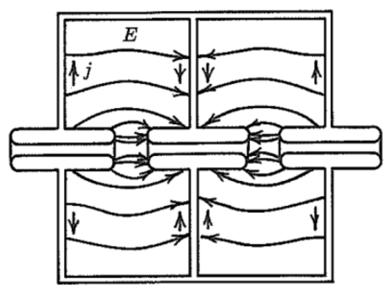
The Side-Coupled-Cavity Linac is the backbone of the LANSCE facility

- **This structure was invented at LANL in the 1960's and is the core of most electron radio-therapy machines (it was never patented)**
- **It is based on the principle of the normal modes of coupled harmonic oscillators where inductance and capacitance are the electrical analogs of the spring-mass arrangement of classical physics**

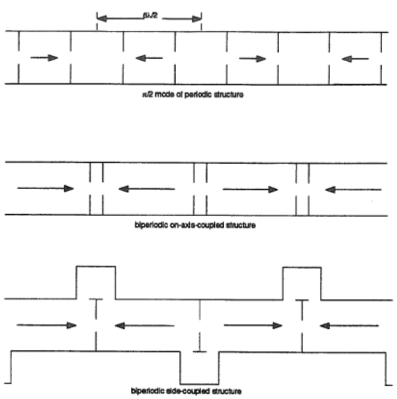




(a)

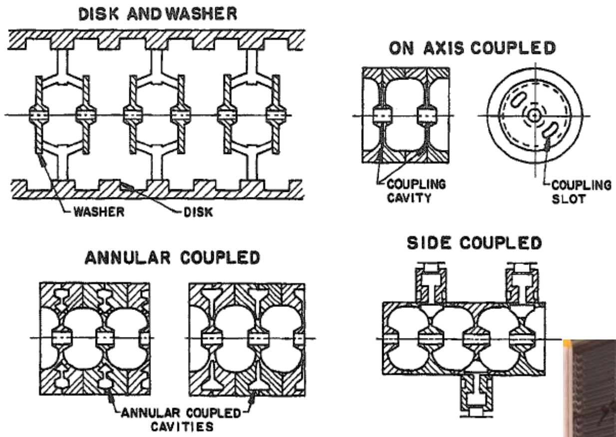


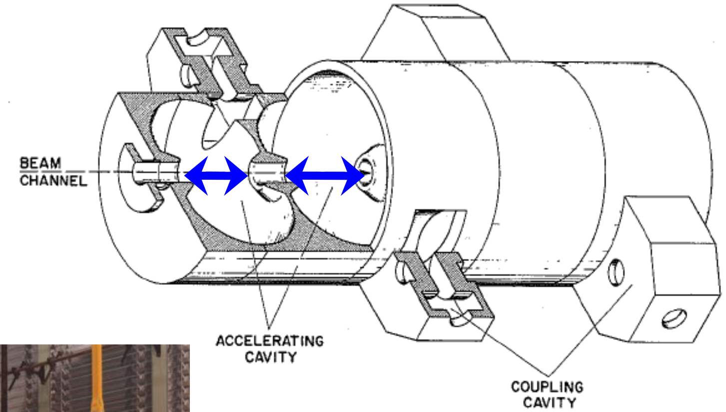
(b)

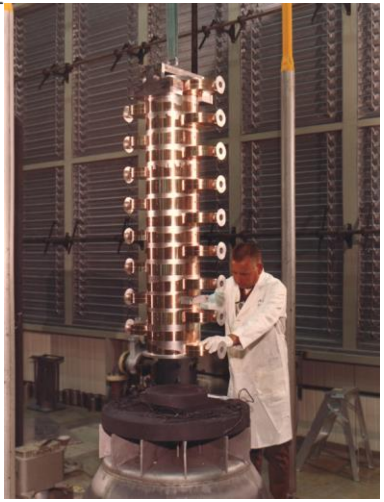


The selection of a particular arrangement is determined by the beam acceleration range, energy gradient and shunt impedance (efficiency) of the structure

- **The π/2 mode with the unexcited cavities off-axis was the optimal structure for efficient acceleration of protons at high power at the time LANSCE was designed**



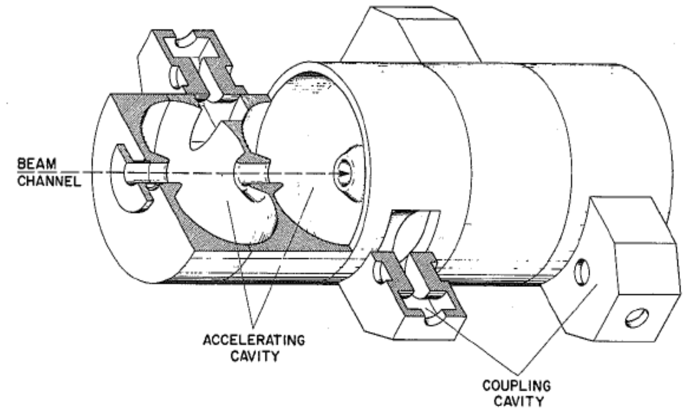




Side-Coupled Linac

- The behavior of the SCL is like a bandpass filter whose center frequency is $f_0 = 805MHz$ and the 3dB bandwidth is

$$f_{3dB} = \frac{f_0}{2Q_L} = \frac{805e6}{2 \cdot 20000} = 20.125kHz.$$

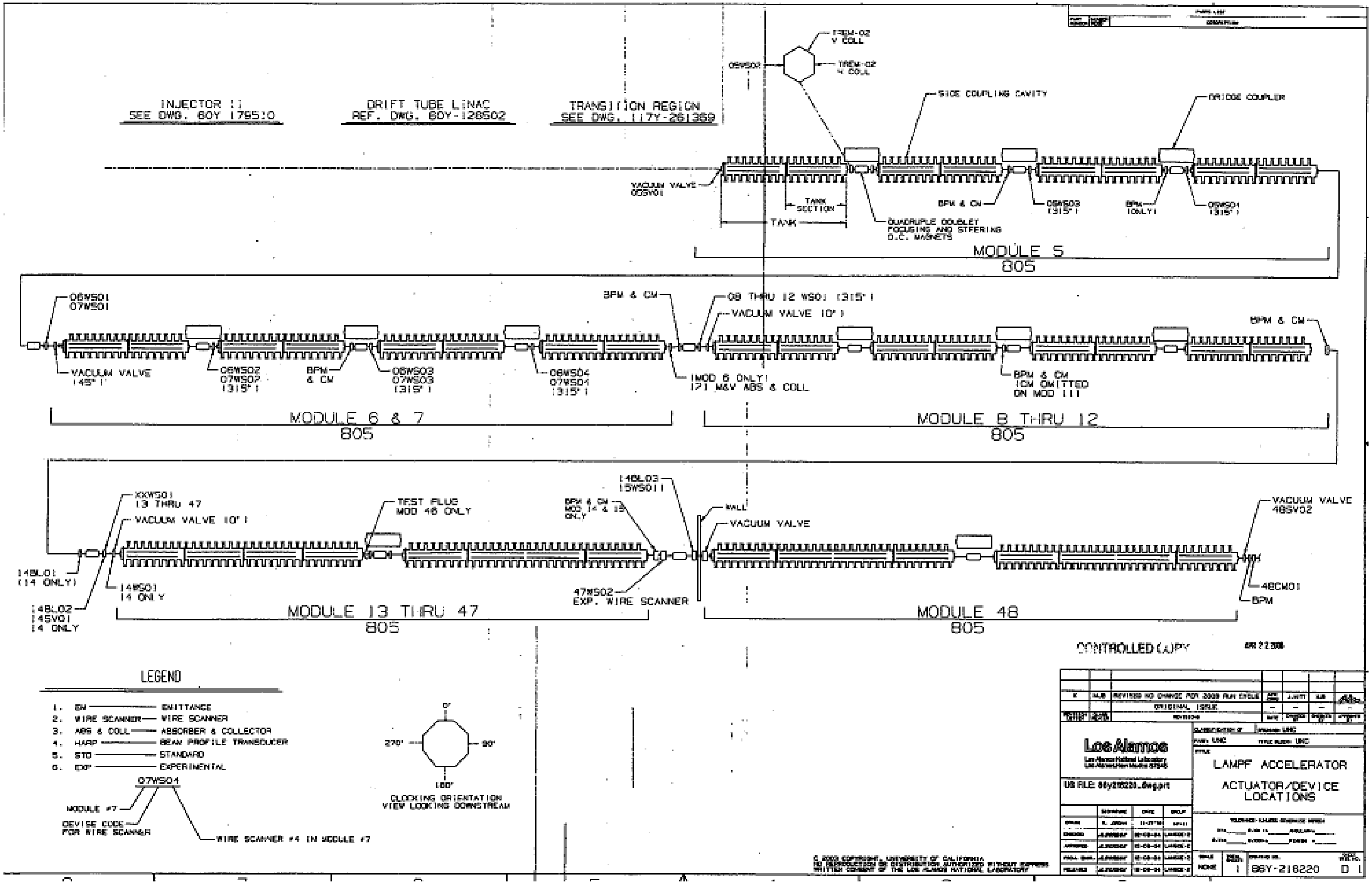


- Instead of working at 805MHz, the dynamics is studied at baseband
- Either amplitude/phase coordinate or Inphase/Quadrature (I/Q) coordinate description is used.
- The baseband dynamics of the SCL in I/Q coordinate is approximated by a stable Two-Input Two-Output system

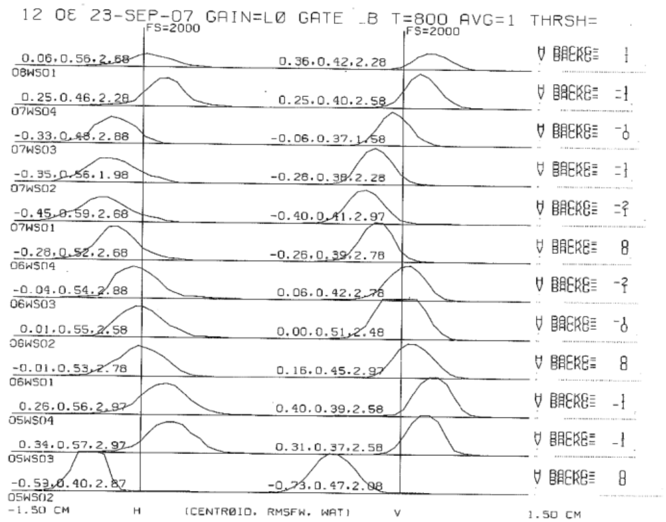
$$G(s) = \begin{bmatrix} g_{11}(s) & g_{12}(s) \\ g_{21}(s) & g_{22}(s) \end{bmatrix} \qquad g_{ij}(s) = \frac{g_{ij0}}{\tau_{ij} s + 1} e^{-s\tau_{dij}} \qquad i, j = 1,2.$$

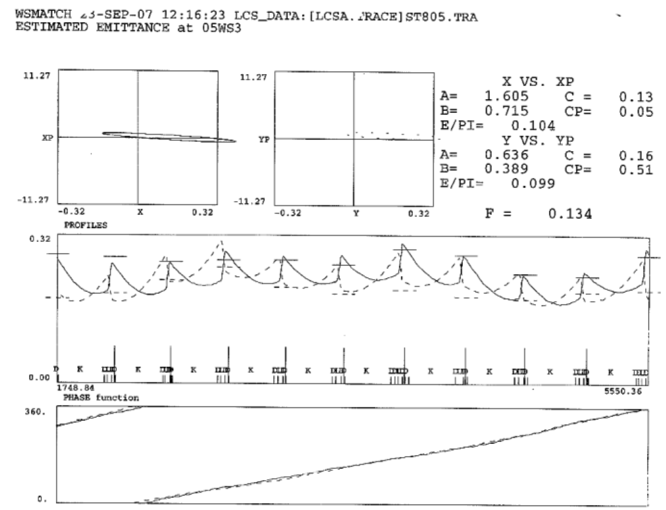
- The gains of Cross-coupling terms g_{120}, g_{210}, are depending on the resonance control performance and very small
- The controller design is approached as if I and Q channels are independent.

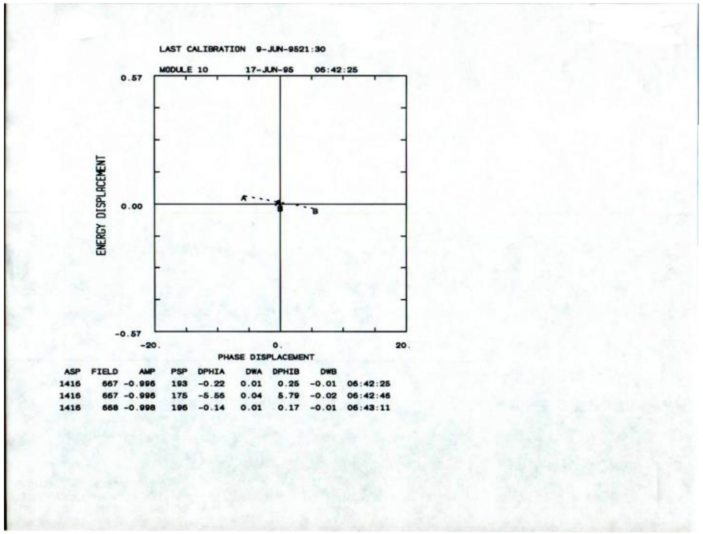
There are 44 accelerating modules, each about 16m long and providing ~16MeV of energy gain; Modules 5-12 have four tanks, Modules 13-48 each have two tanks



Beam matching and proper energy gain for each module in the SCL are important for beam quality

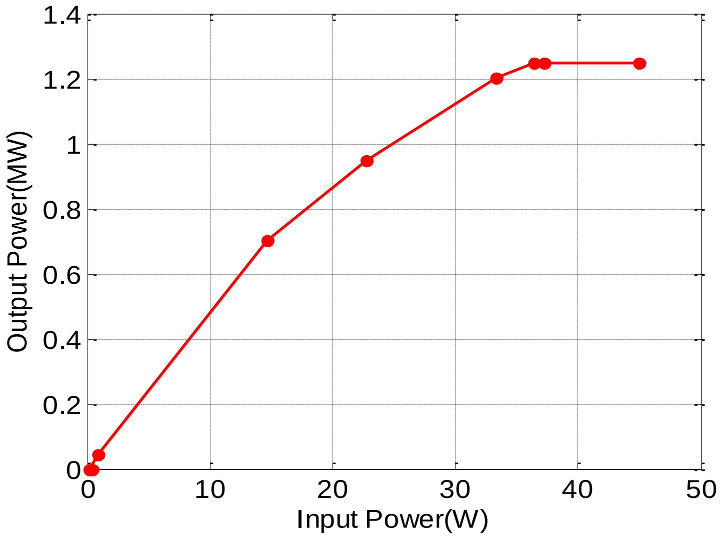


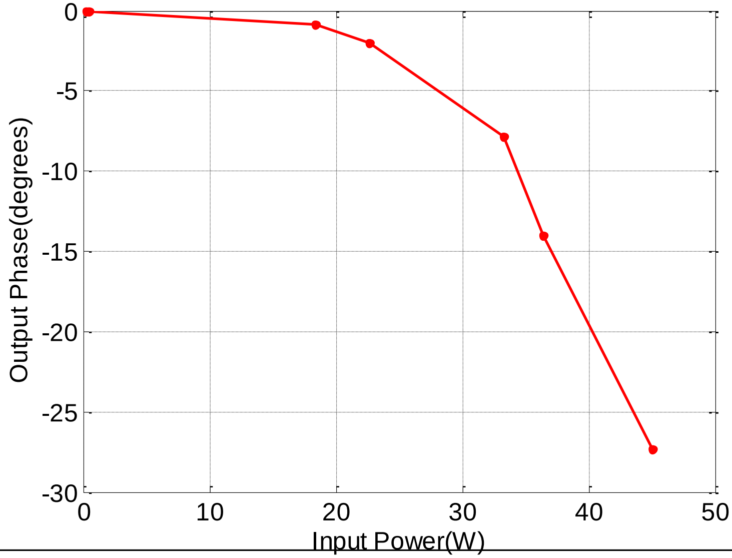




The 805 MHz klystrons at LANSCE (44) are high power RF amplifiers (Max Output Power :1.25MW) in use which have Nonlinear Characteristics

Klystrons in service at LANSCE

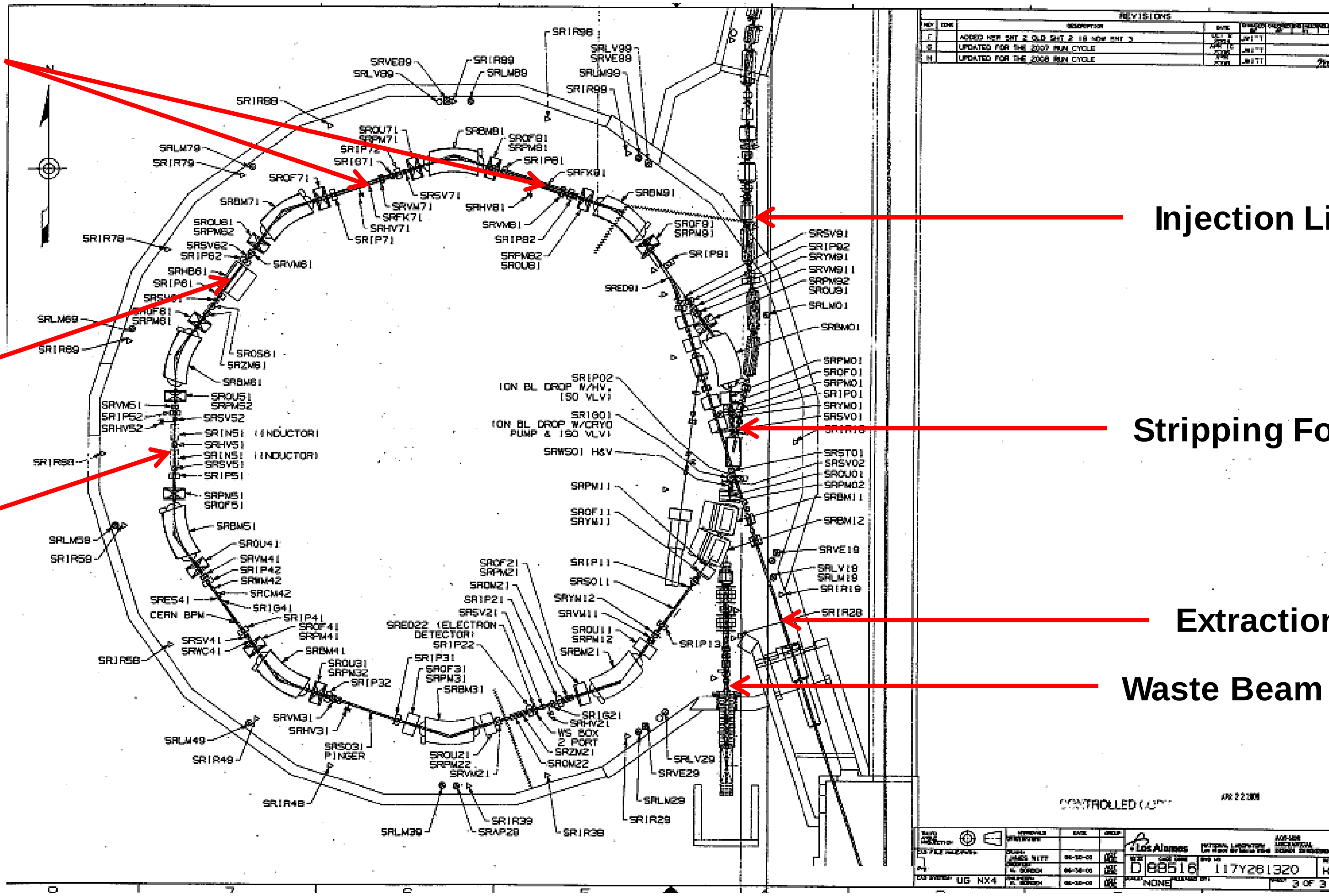




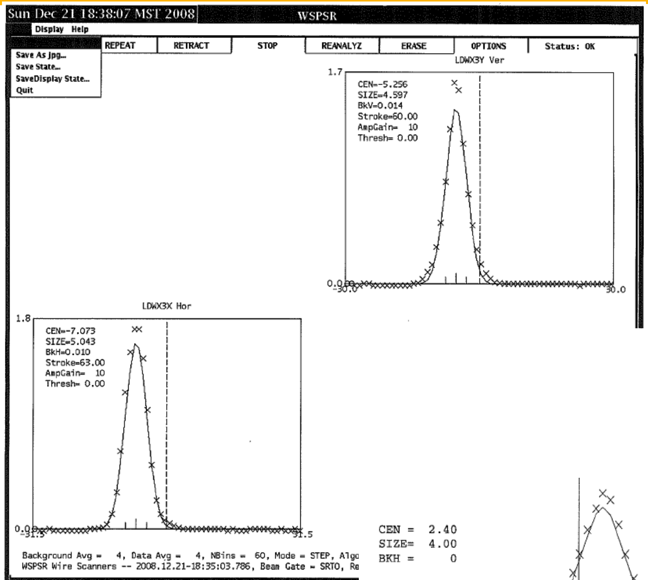
Proton Storage Ring (PSR)

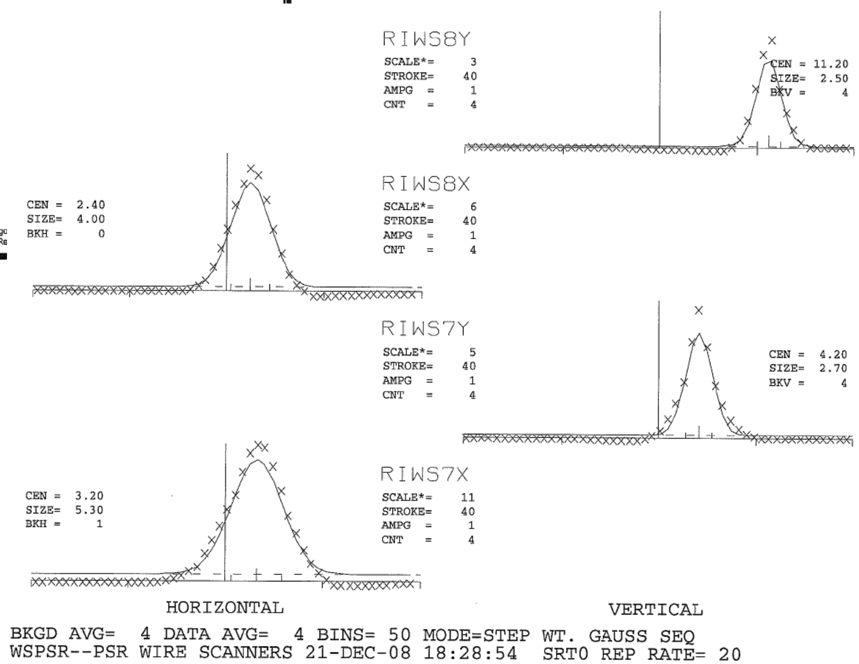
- The PSR is essentially a pulse compressor/charge accumulator
- Recall the chopping pattern imposed in the LEBT with a period of 360 ns – this is the revolution period in the PSR for an 800-MeV proton
- Each sequential ~270ns pulse of H- is stripped by a foil and captured in the ring, and joins other pulses already circulating
- Beam stability is maintained by a 2.8 MHz buncher, inductors, and high-multipole magnets
- Betatron oscillations occur in the x and y planes
- The injected beam is offset and "bumped" in a time-dependent way to minimize instability and space-charge effects
- The PSR is probably the most technically challenging accumulator ring ever built

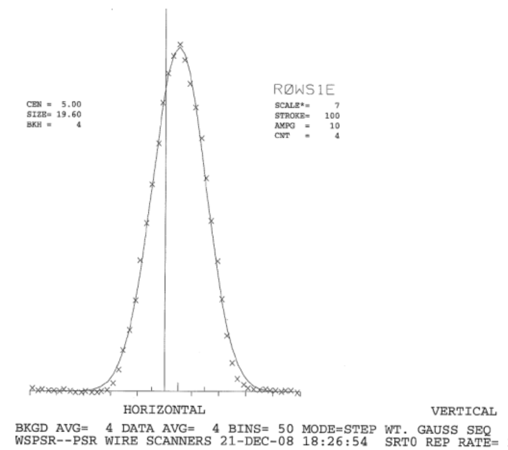
A plan view of the PSR, while complex, does not capture the full complexity of getting the beam into the ring and then out to the target



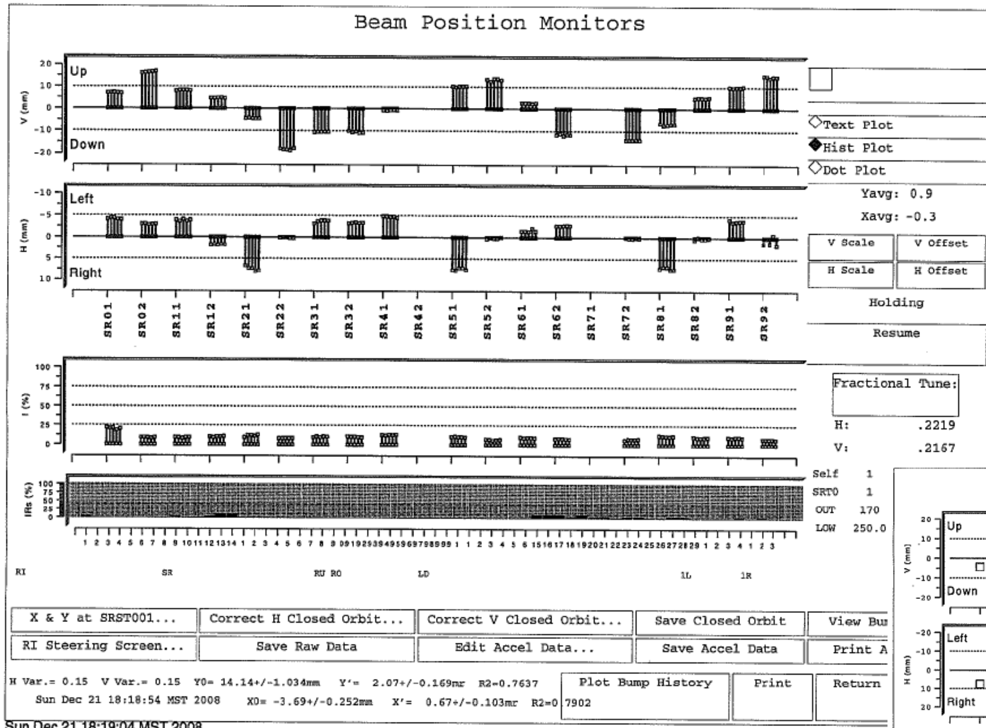
Injection painting and space charge effects cause significant growth in the beam size from injection to extraction



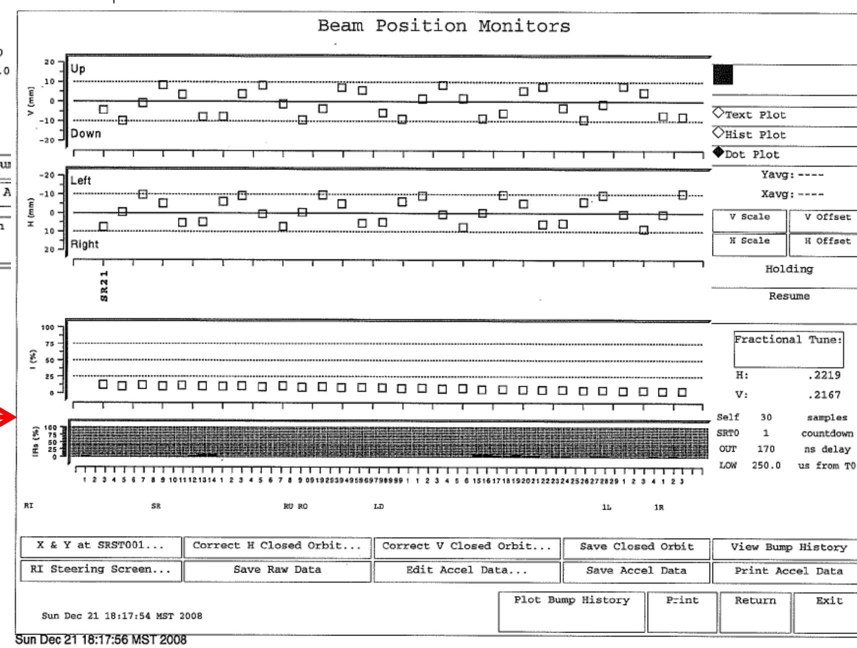




The beam in the PSR oscillates around the closed orbit



This data set shows the oscillation of the beam in both the H and V planes as it orbits the ring – each set of bars corresponds to a beam position monitor, two in each of the ten sectors

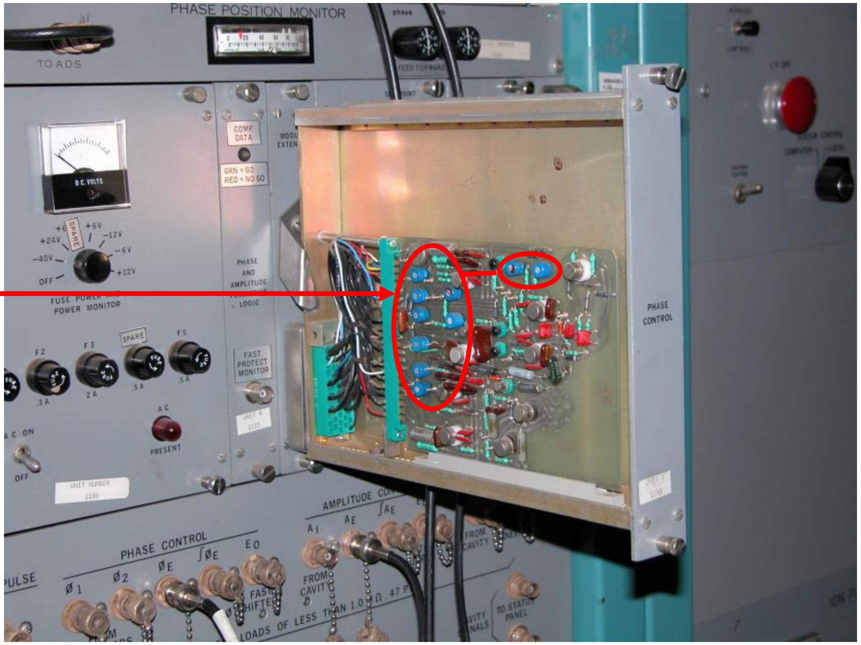


This data set shows the time evolution of the position at a single position monitor and represents the “tune” of the ring

Los Alamos NATIONAL LABORATORY EST.1943

The Low Level RF (LLRF) control system relies upon obsolete technology and lacks modern adaptive capability

- Each of the 96 phase and amplitude control boards in use has up to nine manually-adjustable potentiometers that must be continually "tweaked" to permit stable routine operation
- Phase controls are permanently mounted on extender boards because of the need for frequenct manual adjustment

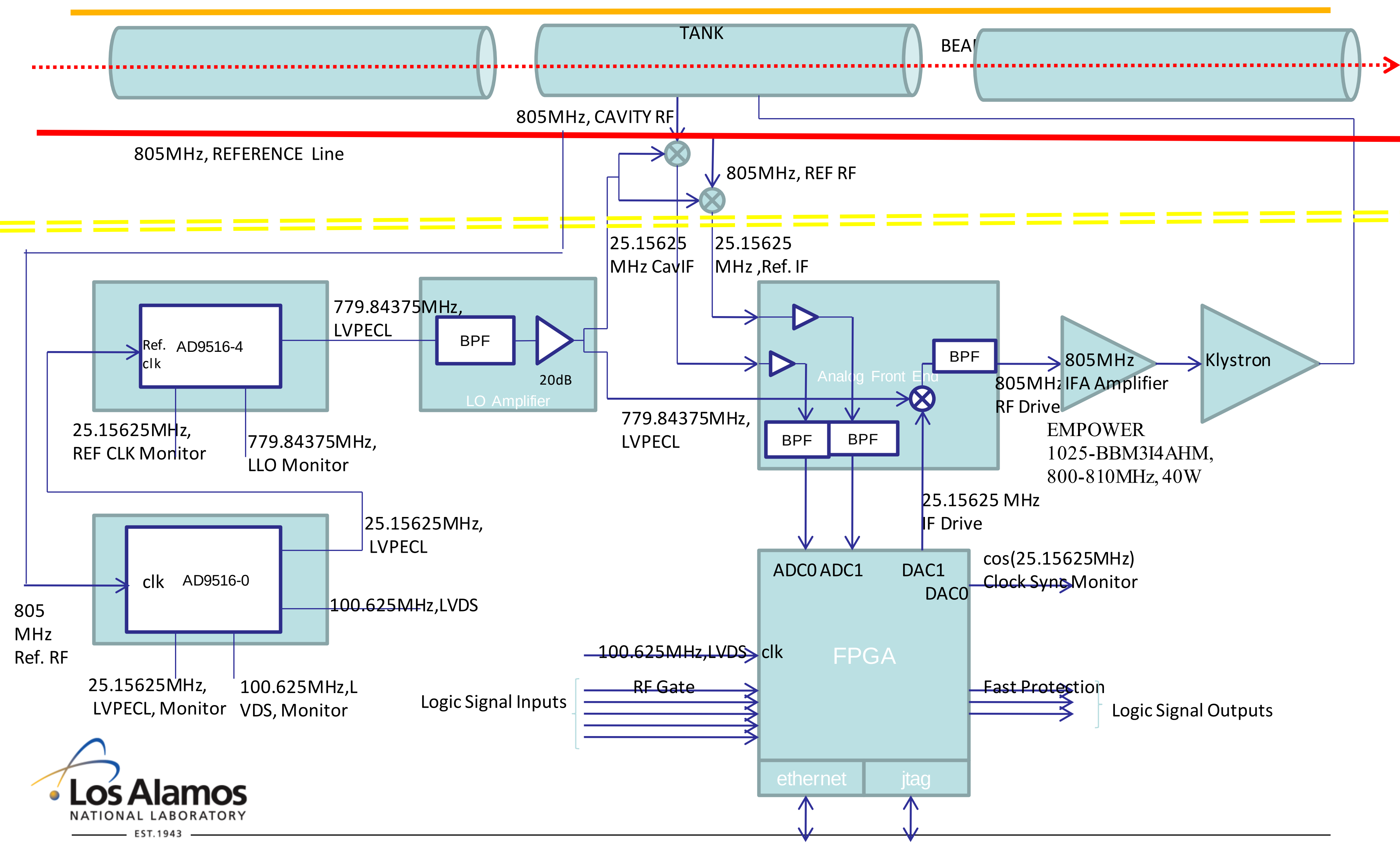


805 MHz phase control card on extender board

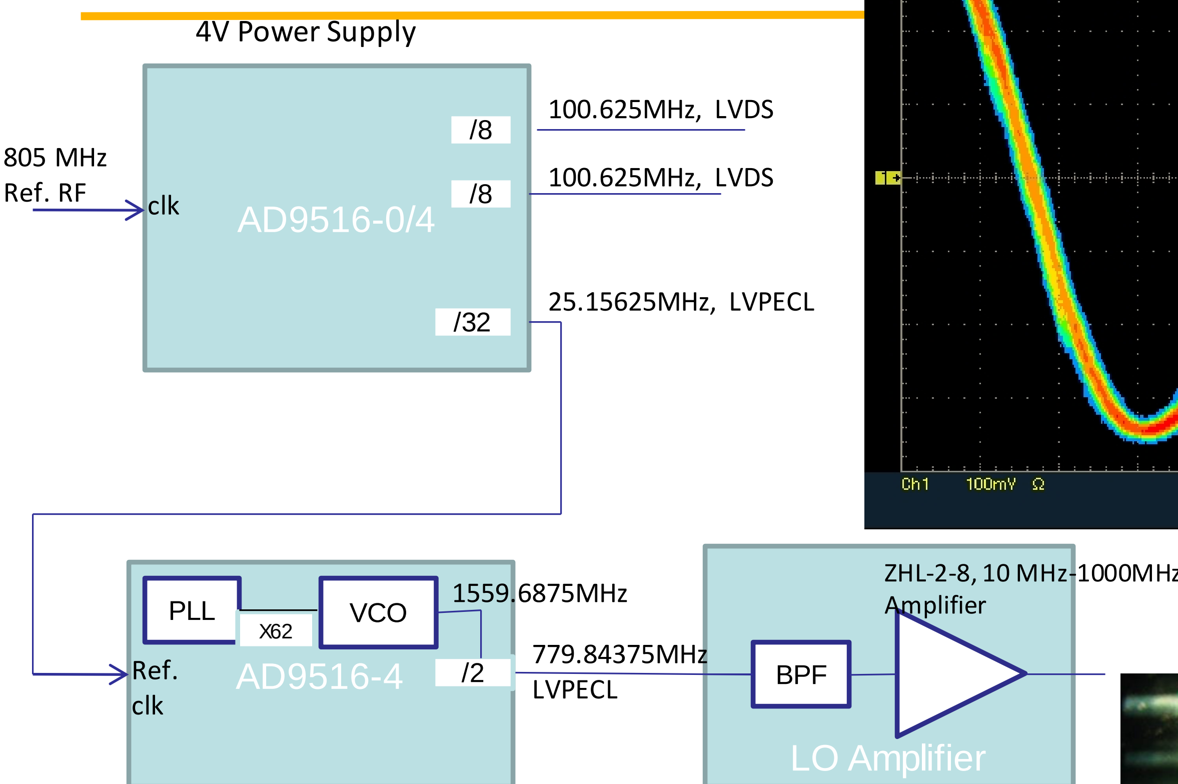
Sector B showing several phase controls

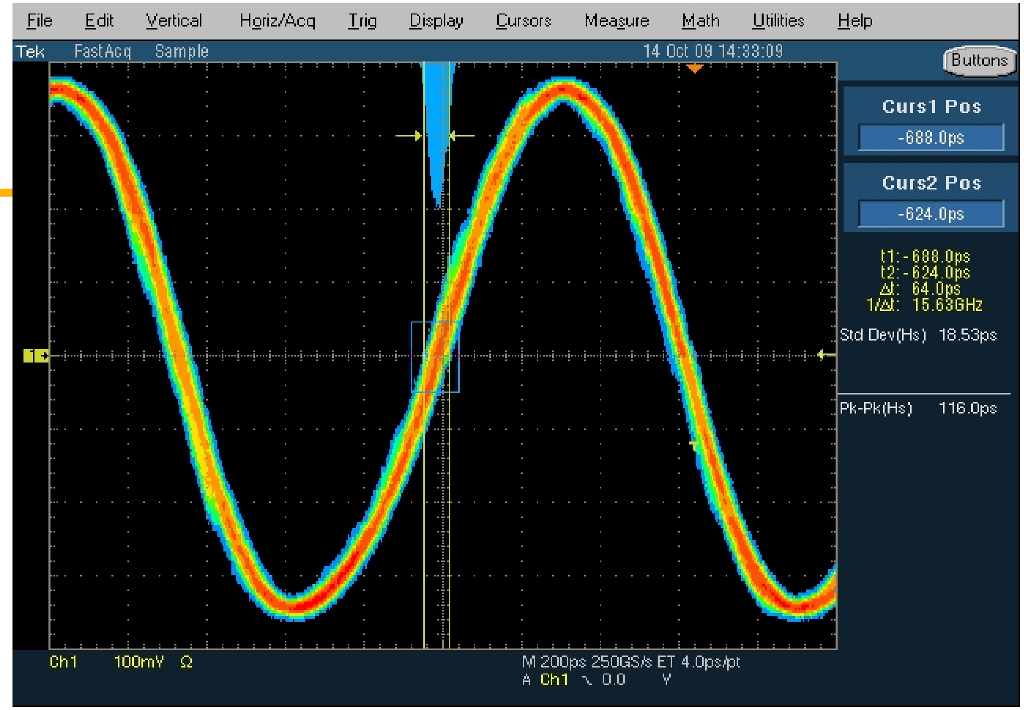
Prototype LLRF SYSTEM

New Low Level RF Feedback Control system is implemented in Altera FPGA

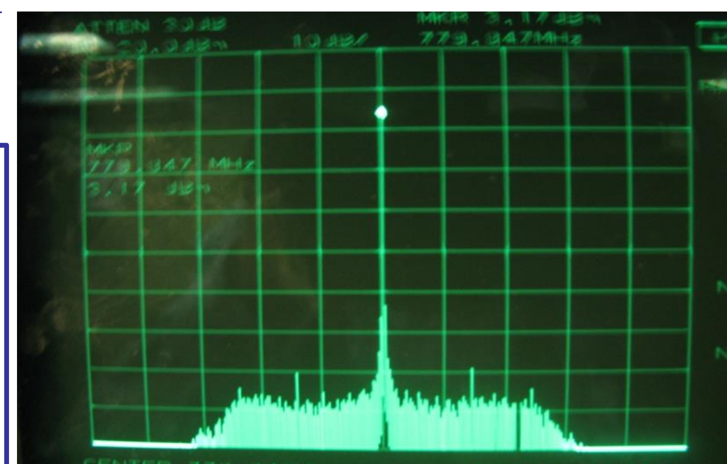


RF/Clock Distribution: Use Analog Devices' Signal generator AD9516



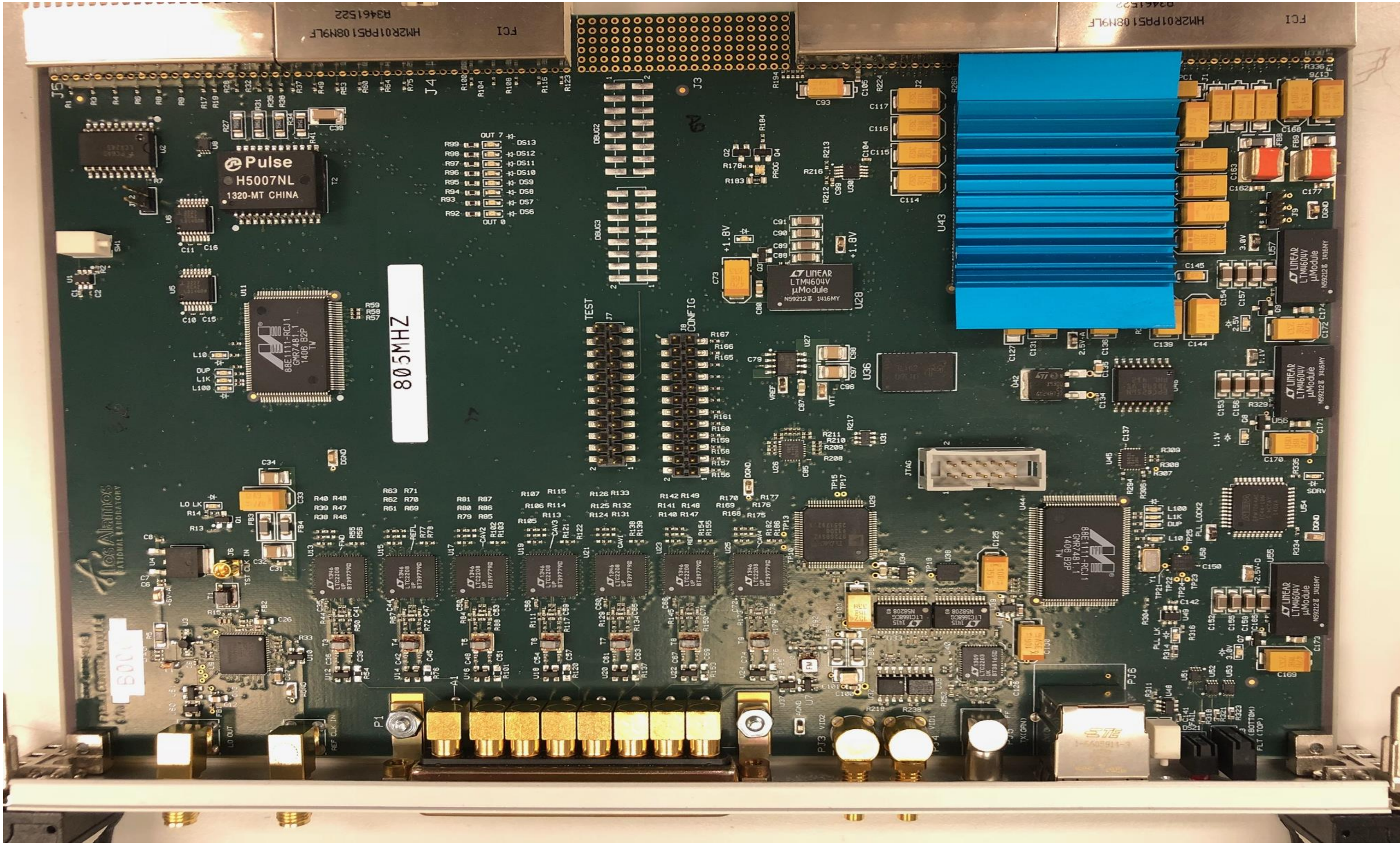


LO (Local Oscillator)

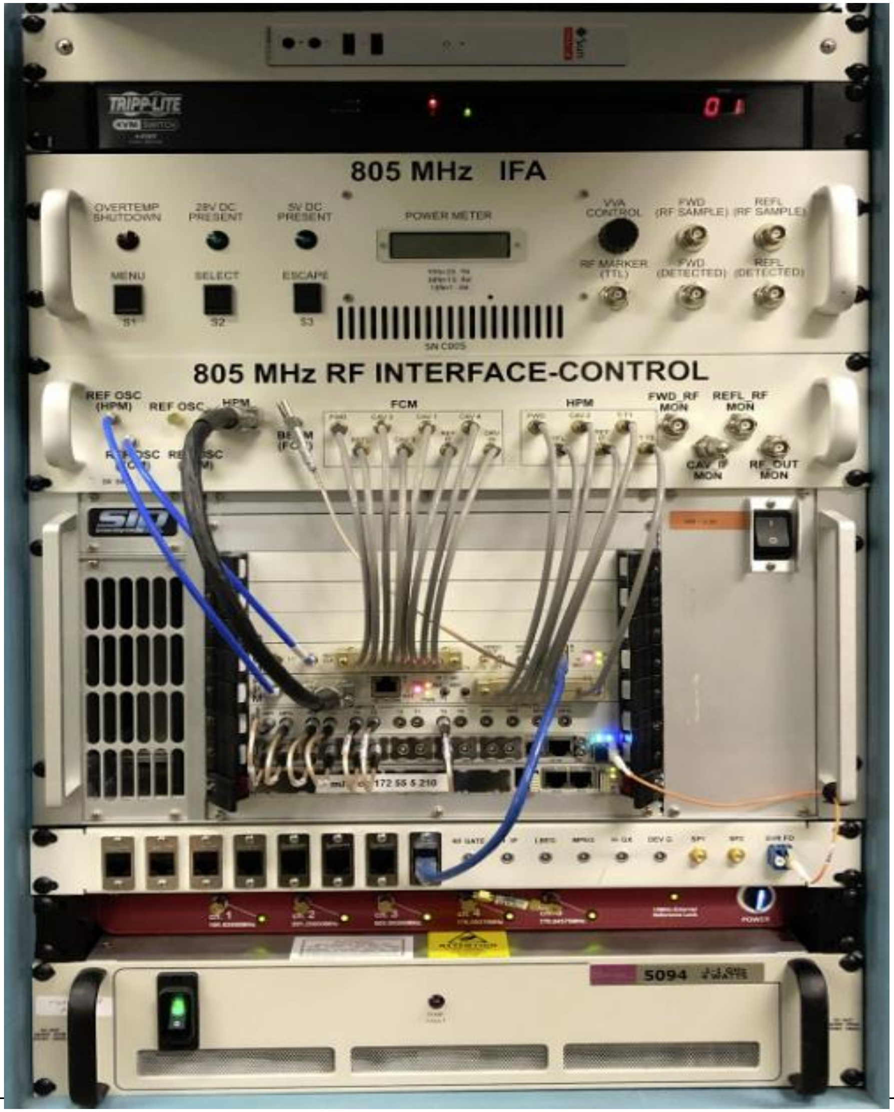


. Two commercial Clock generation boards AD9516 are used
. AD9516 maximum reference clock for internal PLL is 250 MHz, so the second AD9516 is necessary
. For FPGA clock, available 805 MHz reference RF of LANSCE system is used
. The reference clock for the 2nd AD9516 is 25.15625 MHz is generated from the 1st AD9516
. The 4th version of AD9516 is used for the LO (779.83375 MHz) generation
. The internal VCO (1559.6875 MHz) of AD9516-4 is used.
. LO Signal jitter is maintained in the order of few tens ps

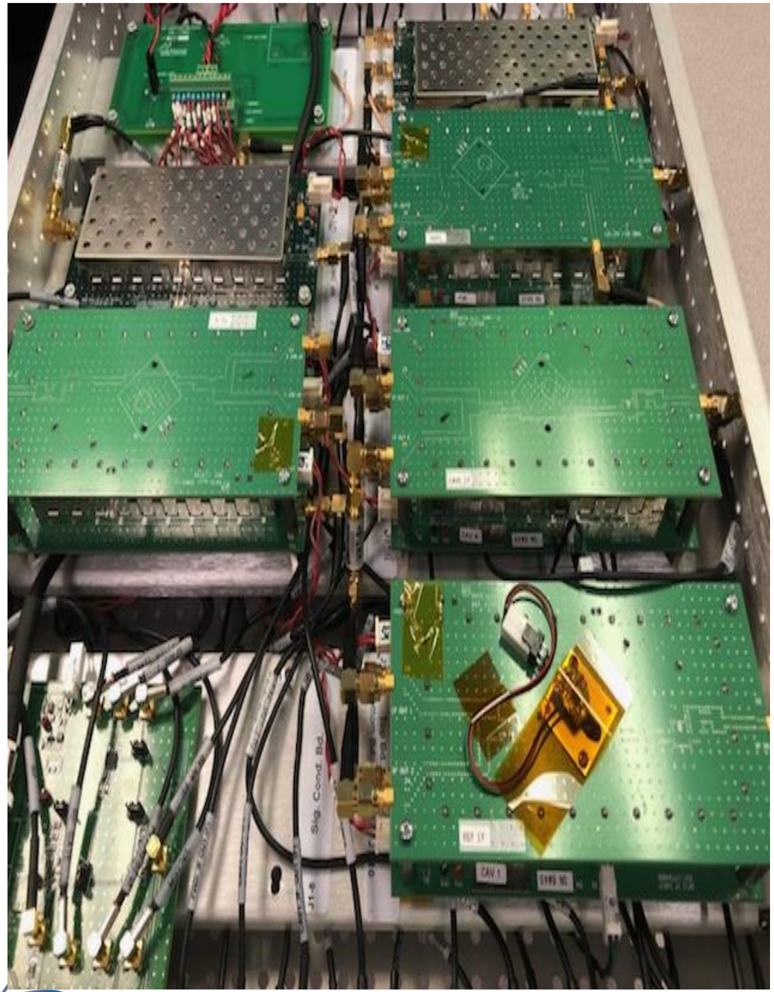
LLRF control system FPGA, ADCs/DACs : Altera Stratix III 3SL260 FPGA board from Altera is used for the prototype Control System Implementation. 7 16bits ADCs and 1 16 bit DACs, 2 16 bit 25MSPS video DACs, 1 16bit 25MSPS BFFADC



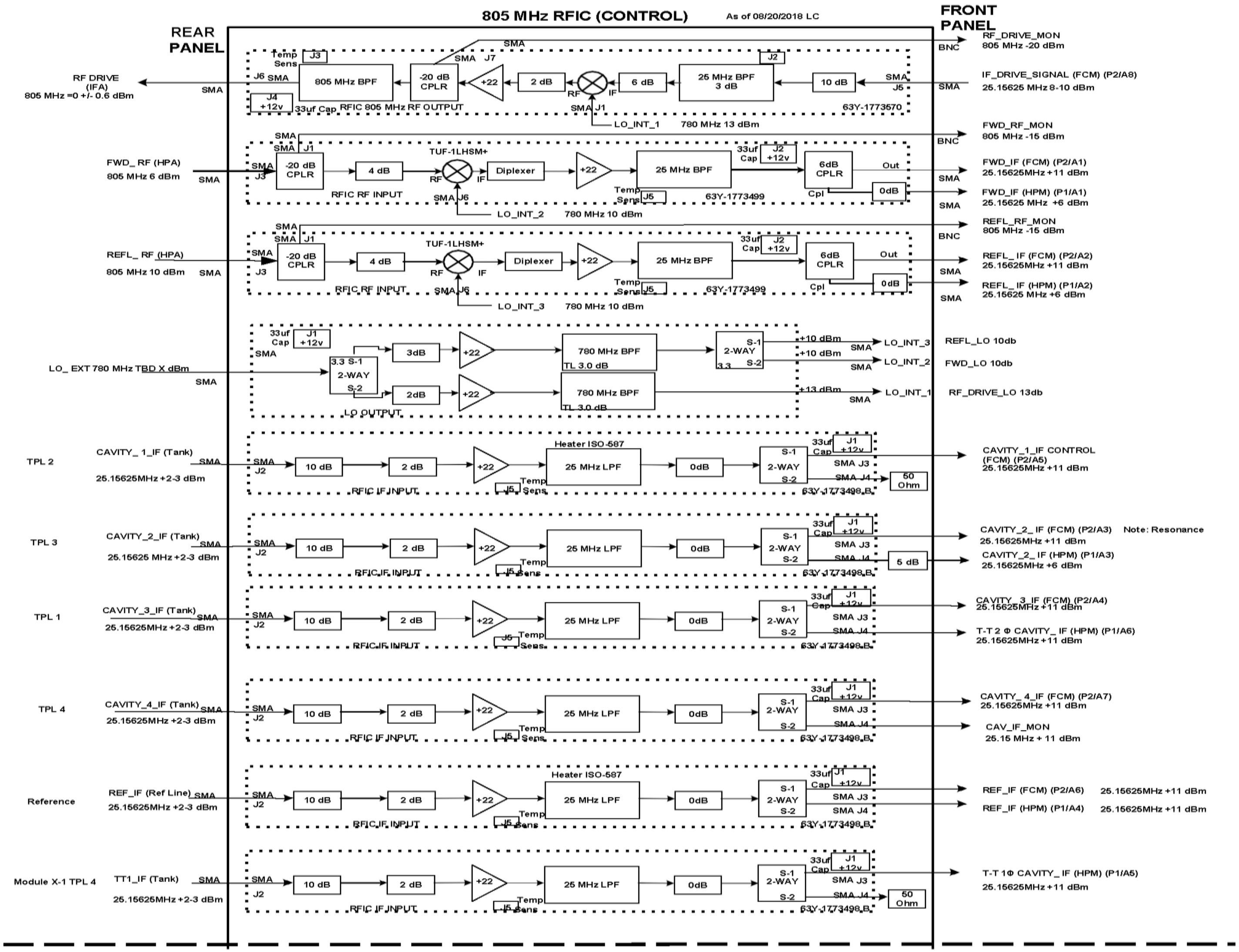
Digital LLRF System



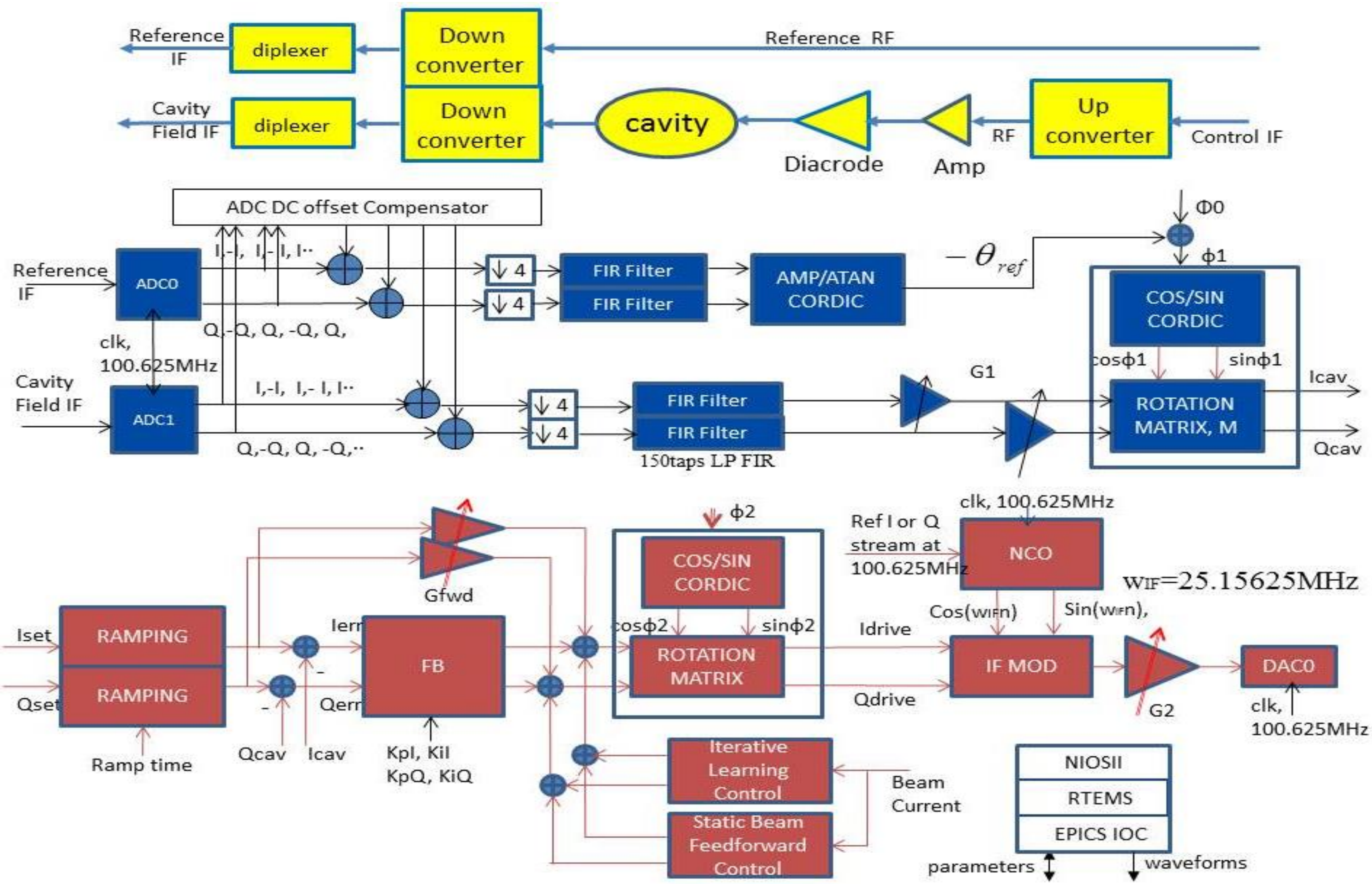
RFIC Boards



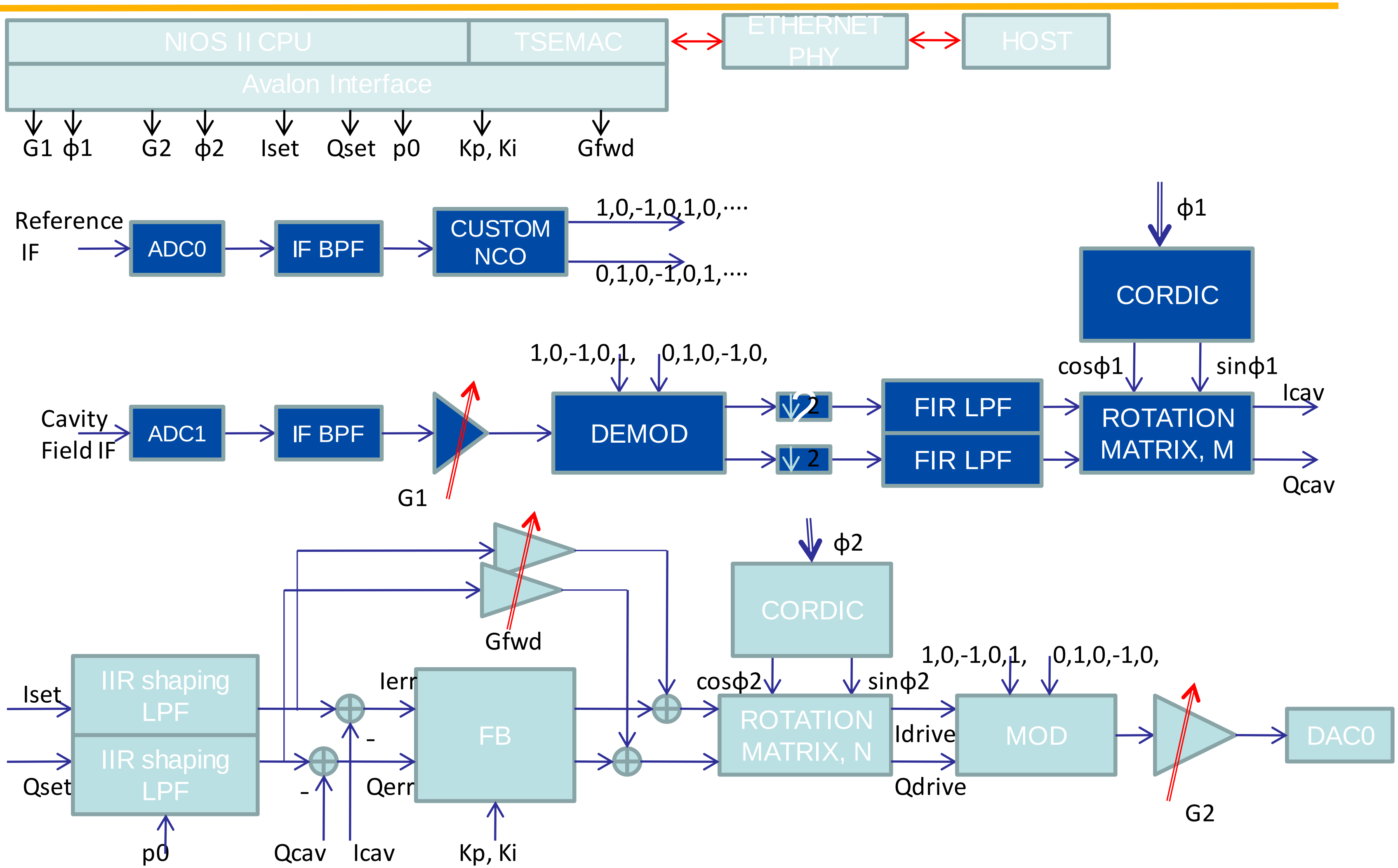
RFIC Block Diagram



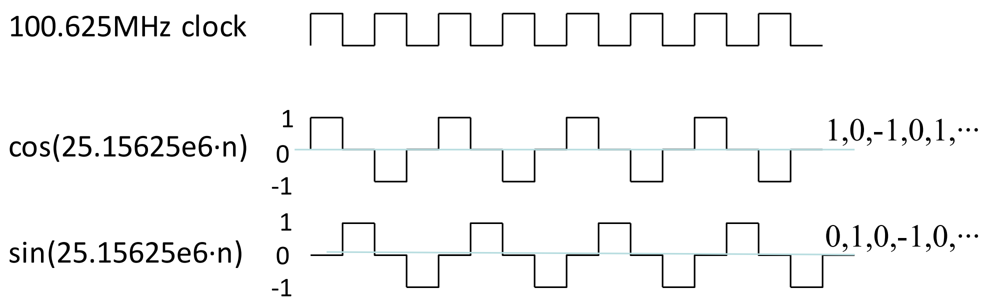
Overall Block Diagram of FCM DSP implemented in FPGA



Receiver Part of LLRF Control System Scheme Implemented in a FPGA : For the rapid prototype HDL generation, DSP Builder is used

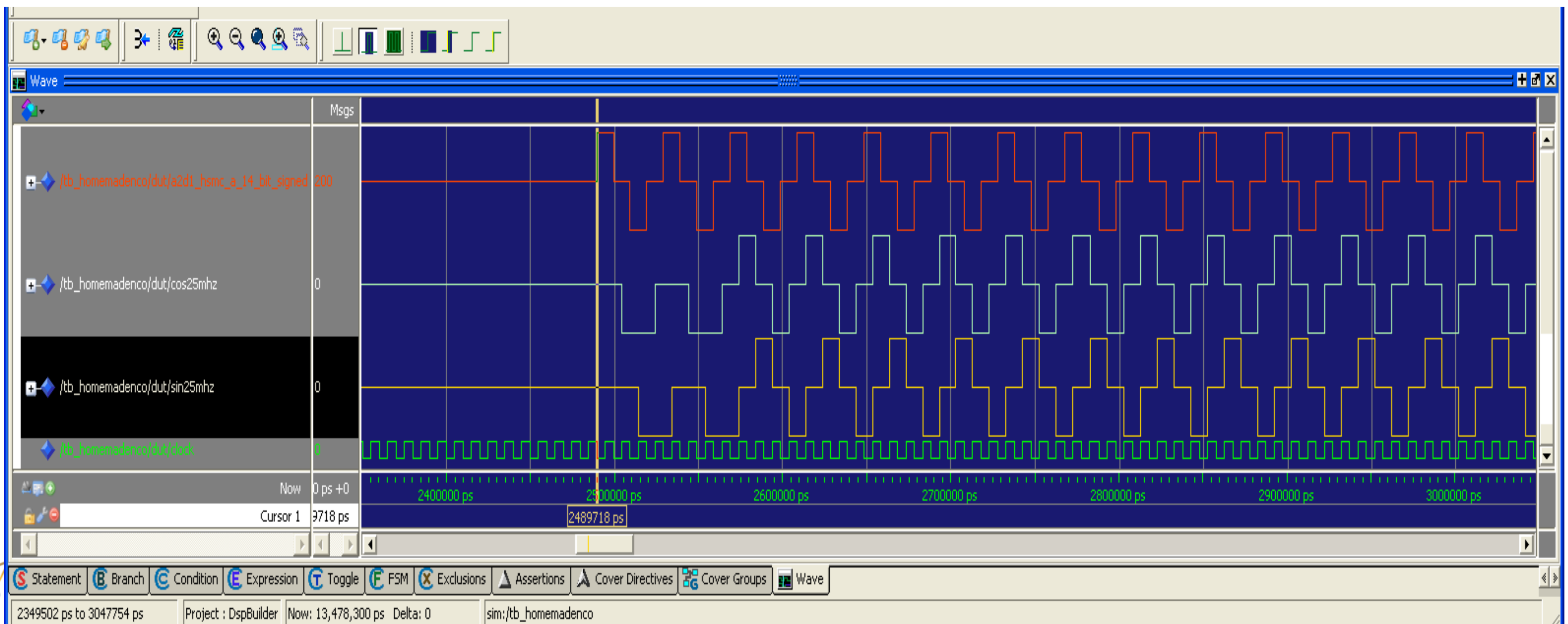


Custom NCO is based on the input reference IF signal, which is synchronized with 805 MHz RF reference and eventually synchronized with 6.28MHz master oscillator signal

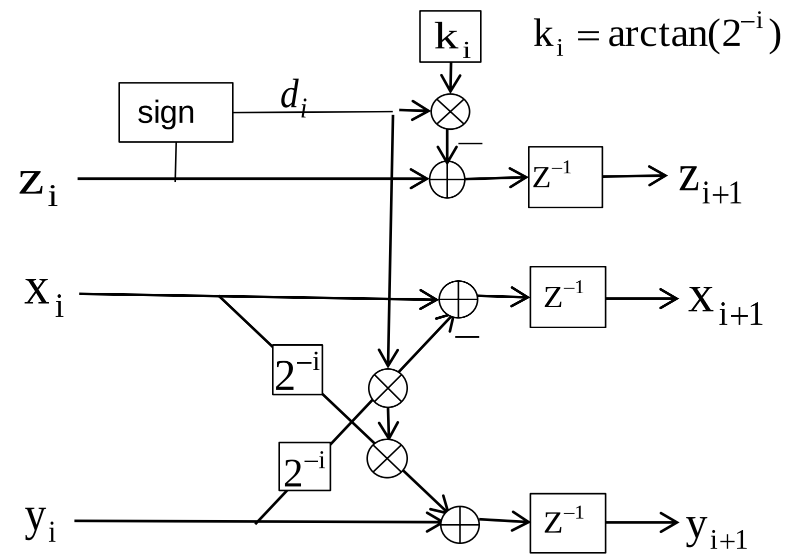


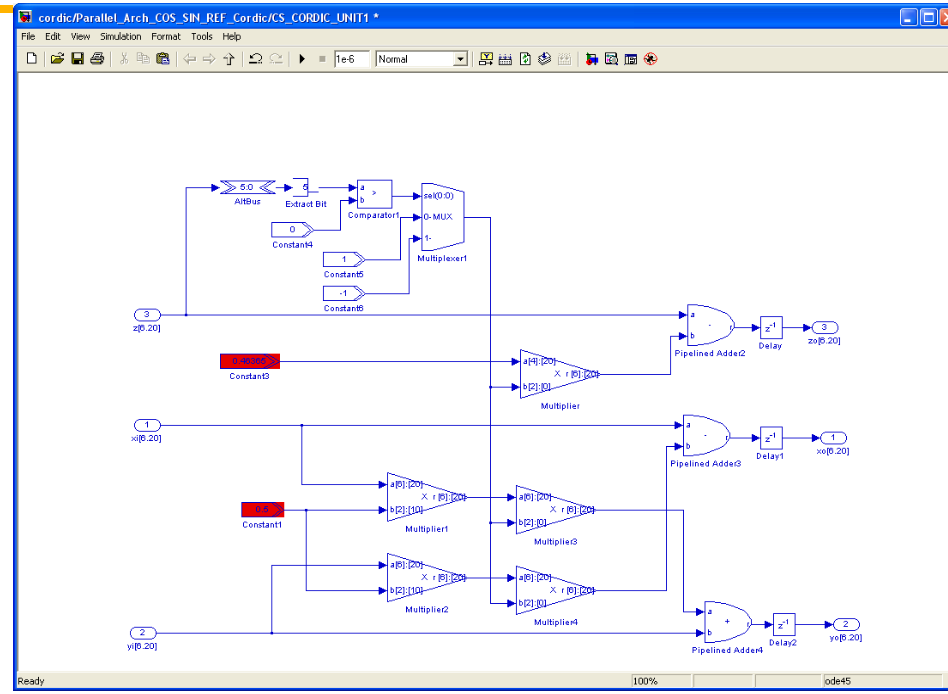
$$F_s = \frac{4F_{IF}}{2m-1}, \quad m = 1,2,\cdots$$

Oversampling



Rotation CORDIC (COordinate Rotation DIgital Computer) : Given input angle, it computes cos and sin of the angle





$$z_{i+1} = z_i - d_i \cdot \tan^{-1}(2^{-i})$$
$$x_{i+1} = x_i - y_i \cdot d_i \cdot 2^{-i}$$
$$y_{i+1} = y_i + x_i \cdot d_i \cdot 2^{-i}$$

ith Stage

$$z_N = 0$$
$$x_N = x_0 \cos z_0 - y_0 \sin z_0$$
$$y_N = y_0 \cos z_0 + x_0 \sin z_0$$

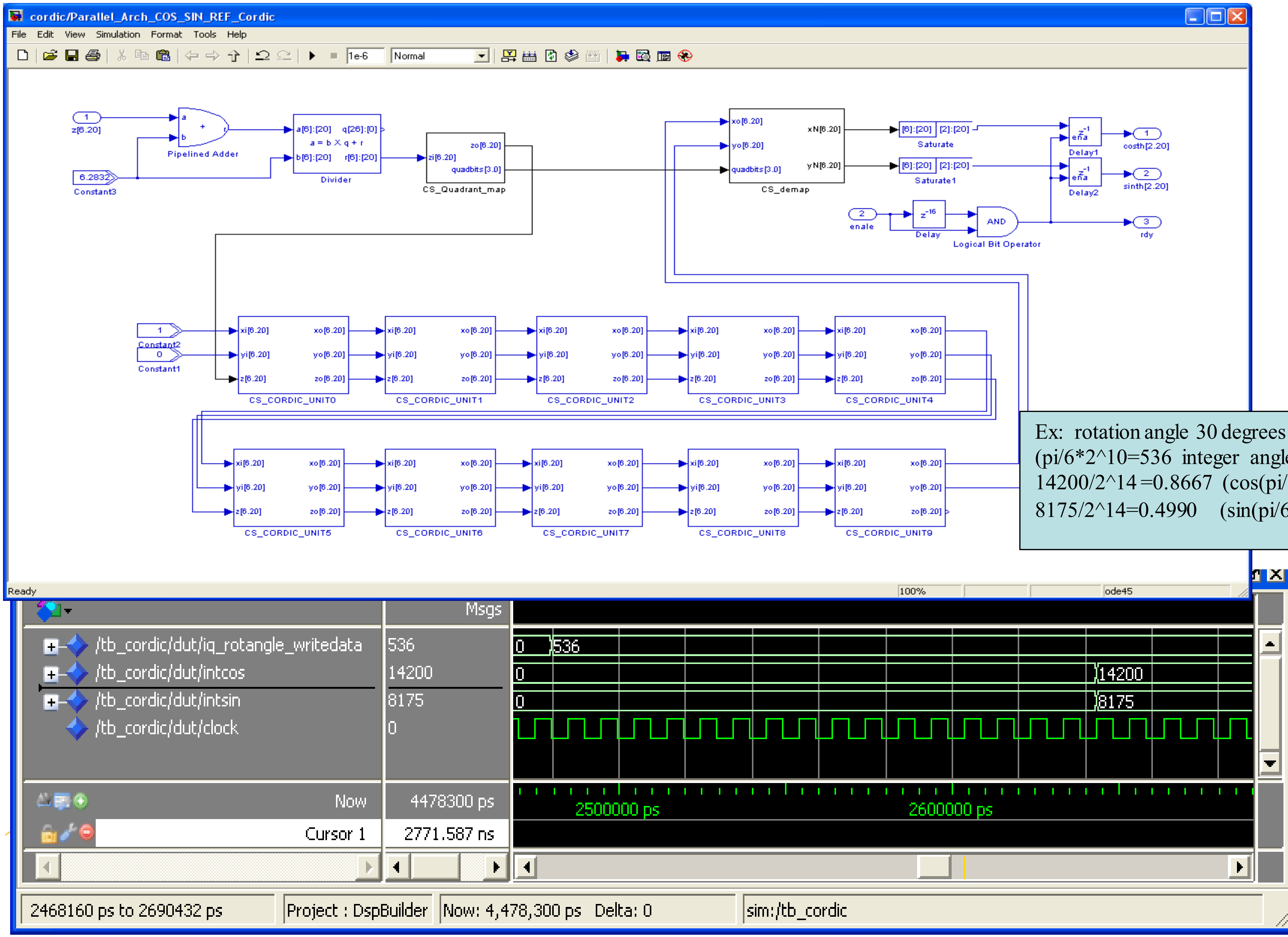
Nth Stage

$$x_N = \cos\phi$$
$$y_N = \sin\phi$$

If 0th Stage inputs

$$x_0 = 1$$
$$y_0 = 0$$
$$z_0 = \phi$$

Rotation CORDIC : 10 Stage DSP Builder Model of CORDIC and Modelsim Simulation



Ex: rotation angle 30 degrees
(pi/6*2^10=536 integer angle)
14200/2^14 =0.8667 (cos(pi/6)=0.8660)
8175/2^14=0.4990 (sin(pi/6)=0.500)

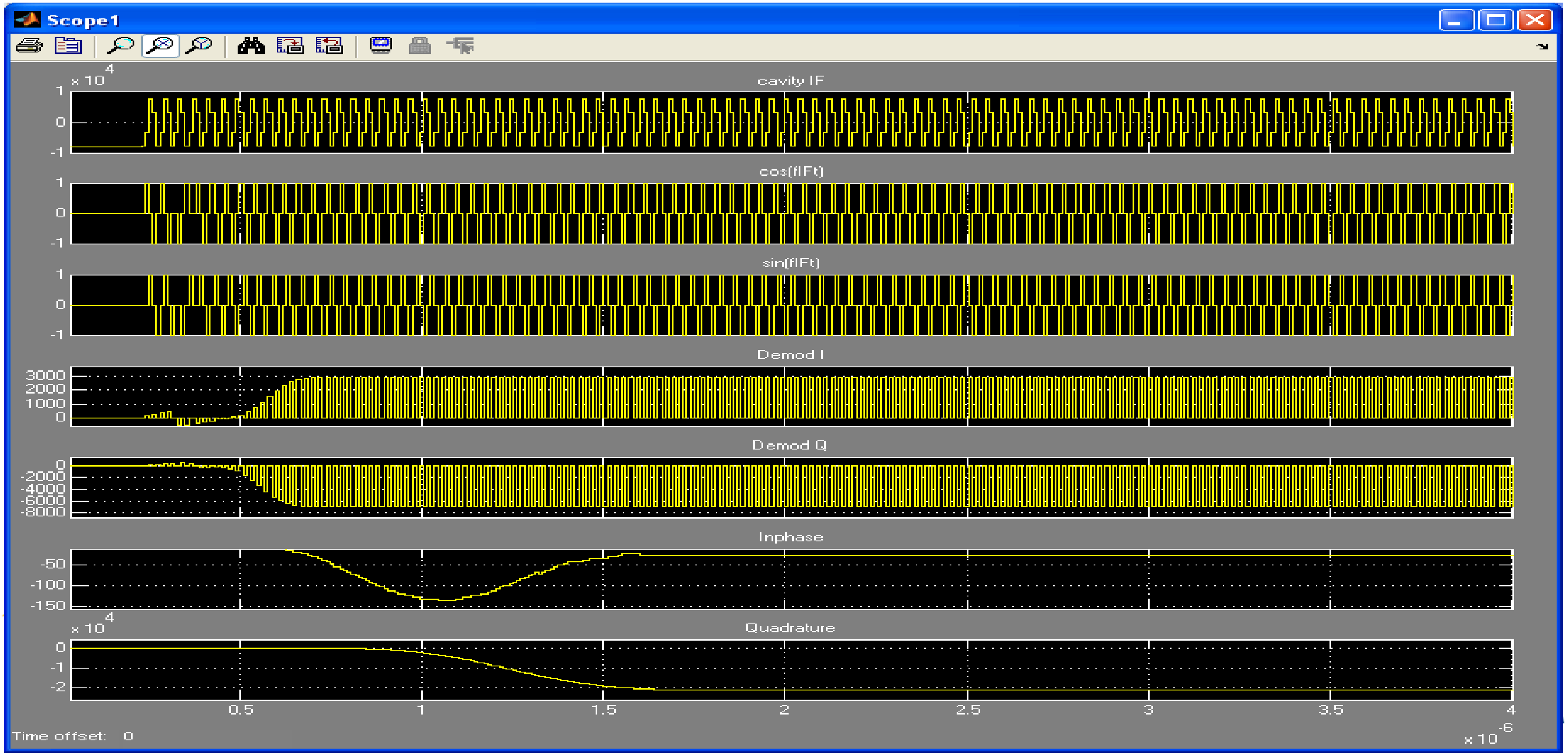
I/Q Demodulation : Because there are 90 taps low pass FIR filters, Base band I and Q outputs see latency

Demod I=Acos (25.15625e6·n+θ) × cos(25.15625e6·n)

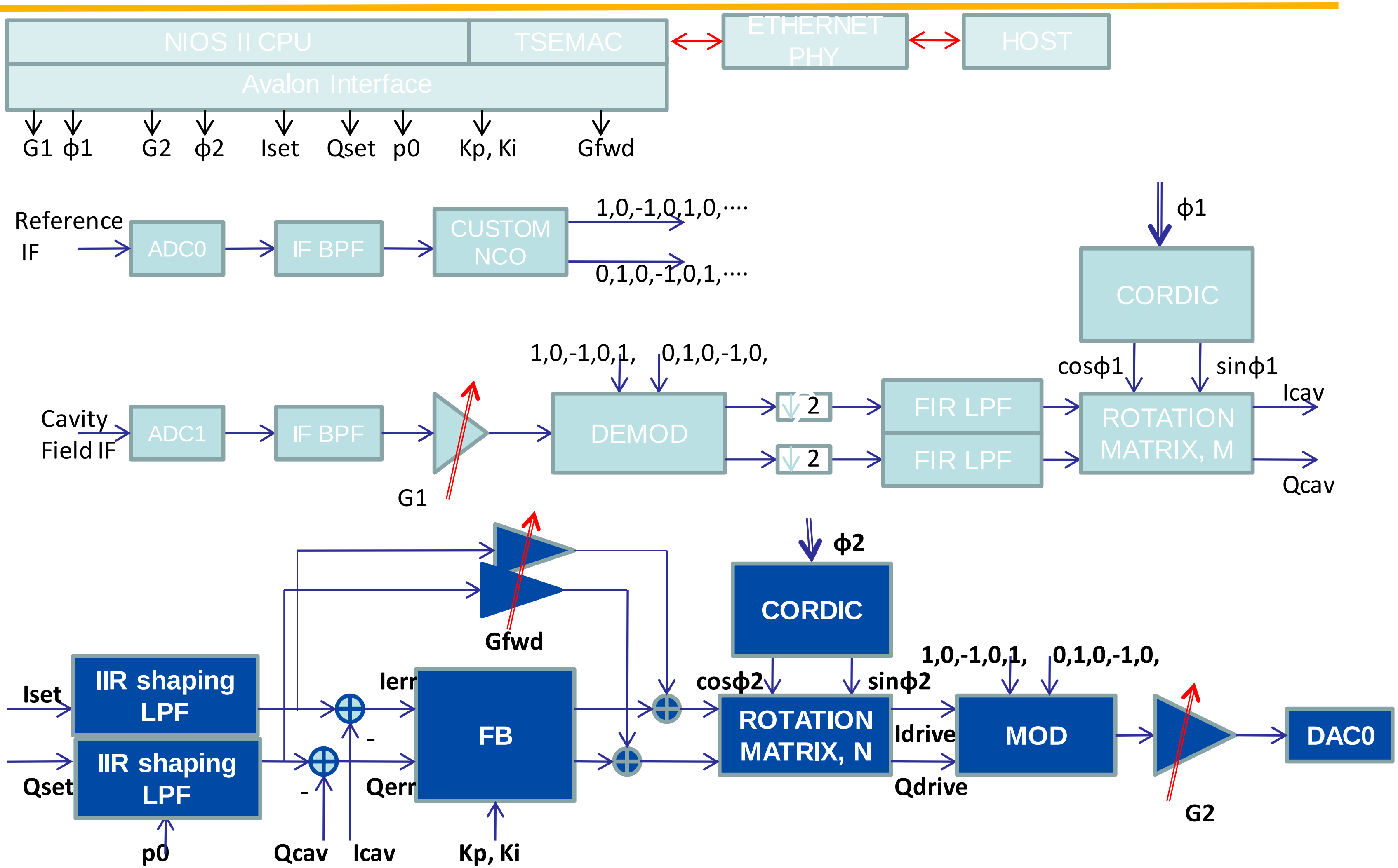
Demod Q=Acos(25.15625e6·n+θ) × sin(25.15625e6·n)

Demod I and Demod Q Signals are filtered by FIR Filters and then Rotated by Rotation Matrix whose elements are output of rotation CORDIC

$$M = \begin{bmatrix} \cos(\phi_1) & -\sin(\phi_1) \\ \sin(\phi_1) & \cos(\phi_1) \end{bmatrix}$$



Transmitter Part of LLRF Control System Scheme Implemented in a FPGA : For the rapid prototype HDL generation, DSP Builder is used



PI Controller:
I and Q channel Controllers are designed in parallel and use the same Gains. Two multiplier and two adders are required for each controller.

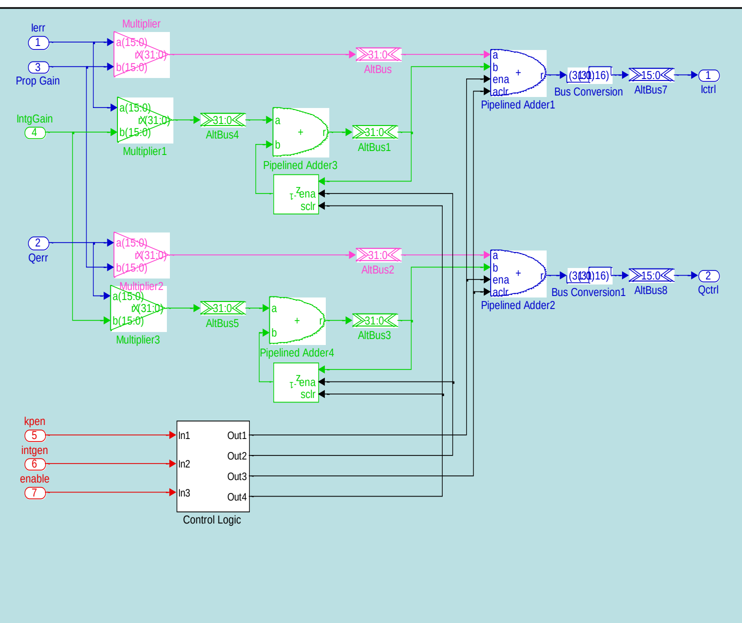
$$u(n+1) = K_p e(n) + K_i \sum_{j=0}^{n} e(j)$$

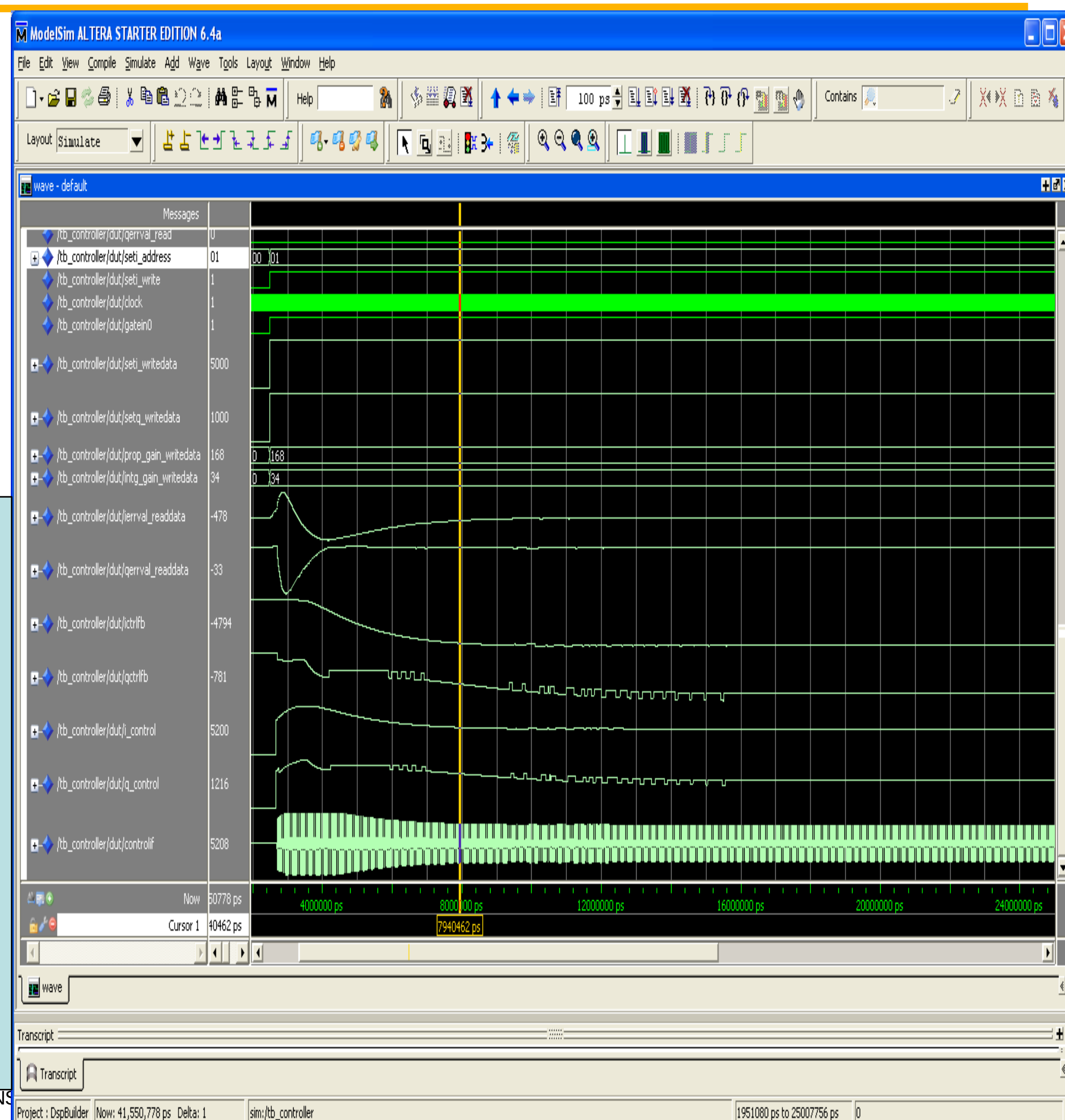
$$= K_p e(n) + u_I(n)$$

$$u_I(n) = u_I(n-1) + K_i e(n)$$

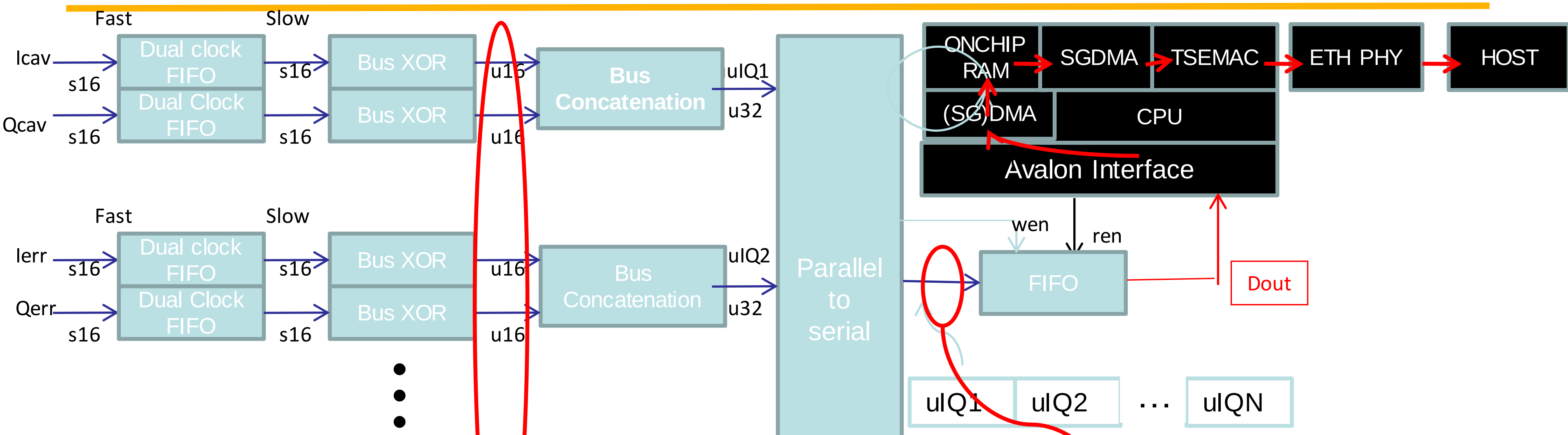
$$u_I(0) = 0$$

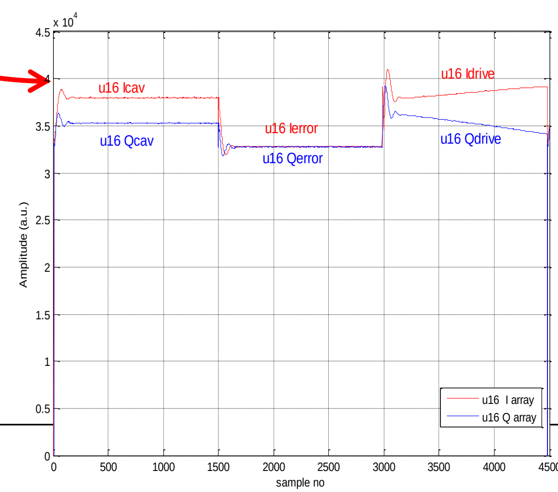
$$C_D(z) = \frac{K_P}{2^{13}} + \frac{K_I}{2^{15}} \frac{1}{1 - z^{-1}}$$

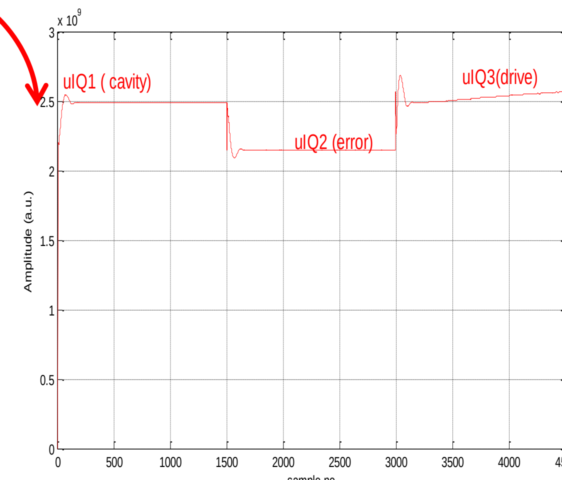




Ethernet Interface : Since only one PHY is provided and several channel data at 100.625 MHz sample rate are to be transferred, data downsampling and data packing is performed using Dual Clock FIFO







.Dout is transferred to the ON CHIP memory using (SG)DMA, whenever data is requested from the Avalon Interface
.Clock rate of the dual clock FIFO is programmable (though needs recompiling)
.Clock rate determines the data size to be transferred

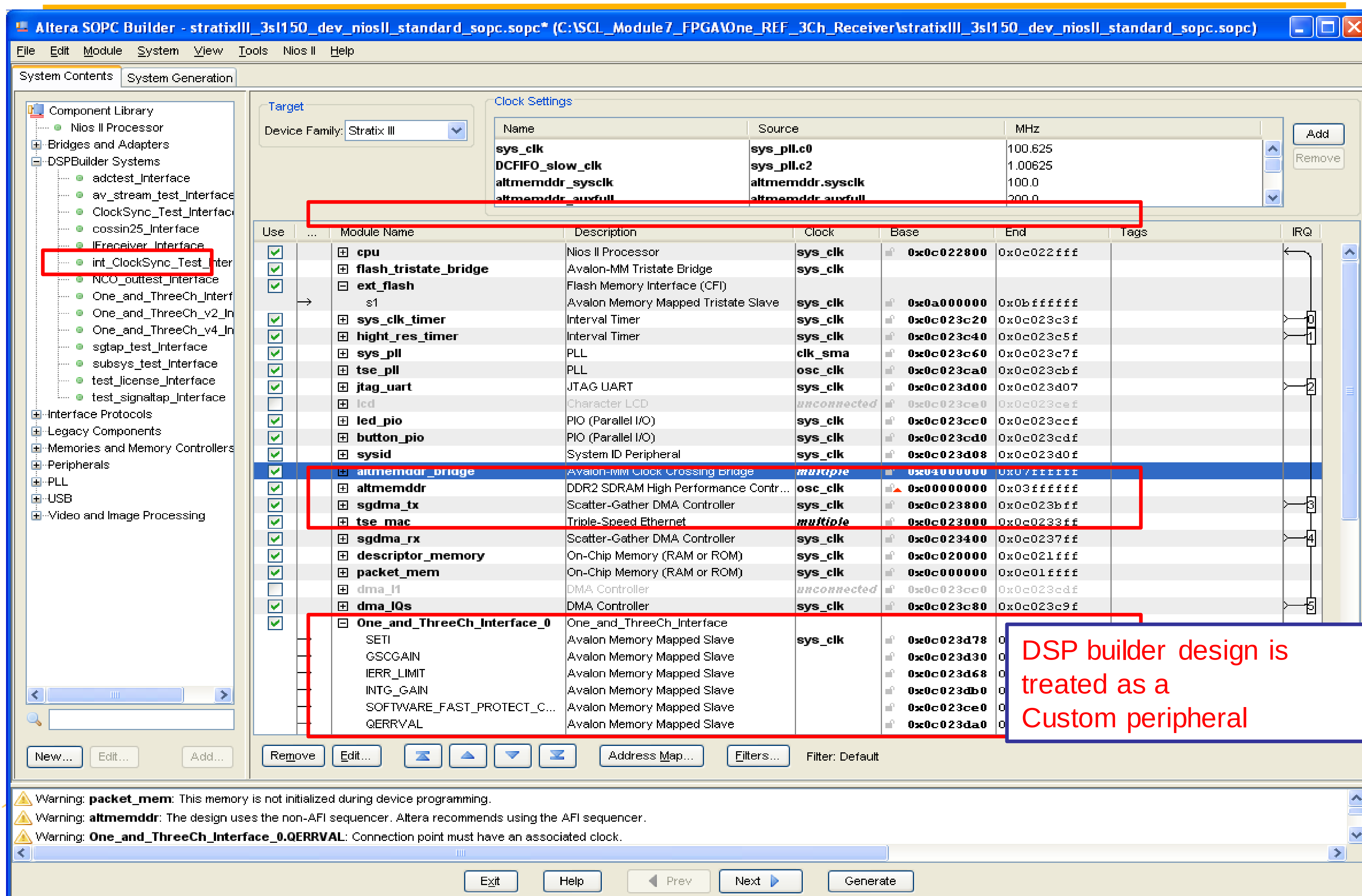
Extracted data from the ethernet uploaded data plotted by matlab

NIOS II Softcore Processor

- 32bit RISC processor
  - Logic Elements, Internal Memory, Hardware Multipliers, Cache are reconfigurable
  - Support Custom Instruction

  – Initialize parameters
  – Decode data from host client and write parameters to the memory mapped registers
  – Read and write parameters from and to the memory mapped registers
  – Initiate DMA, SGDMA
  – Initialization and Data uploading/downloading of network
- TCP/IP STACK
  – Support TCP/IP, UDP socket server/client
  – TSE MAC support : Drivers, library

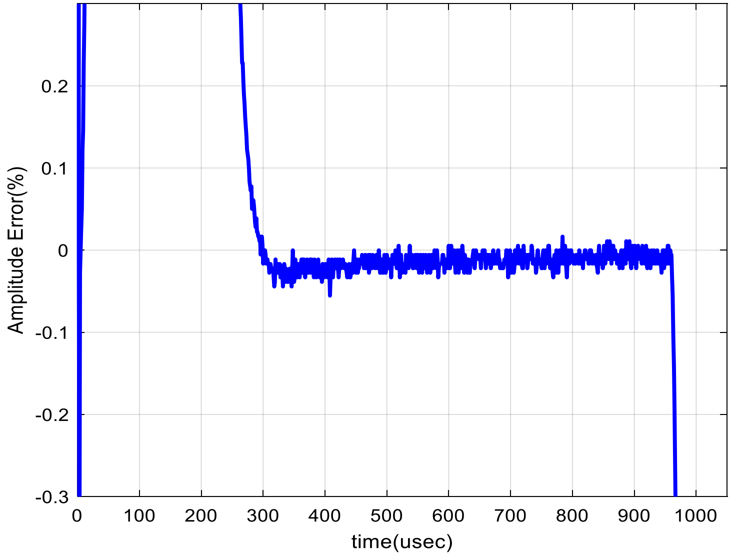
SOPC (System-On-a-Programmable-Chip) Builder System Design: Integrate System On Chip Components (CPU, Memories, Peripherals, Ethernet MAC, etc.)

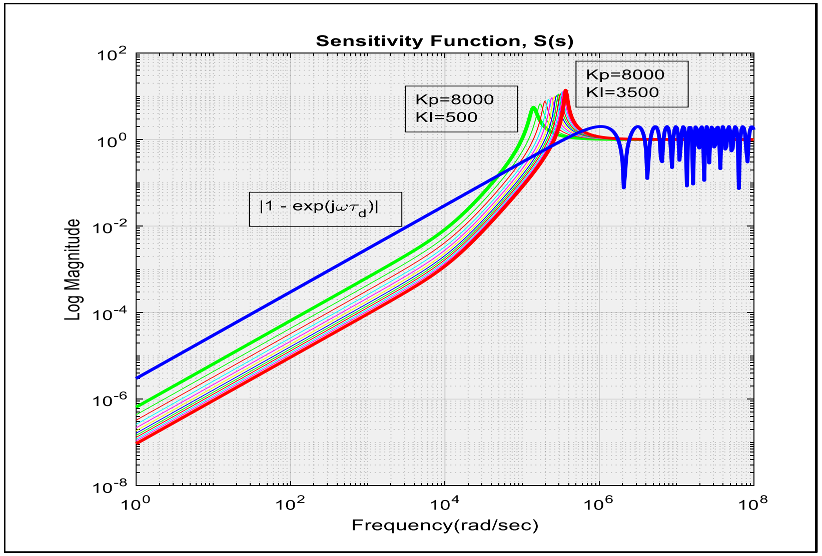


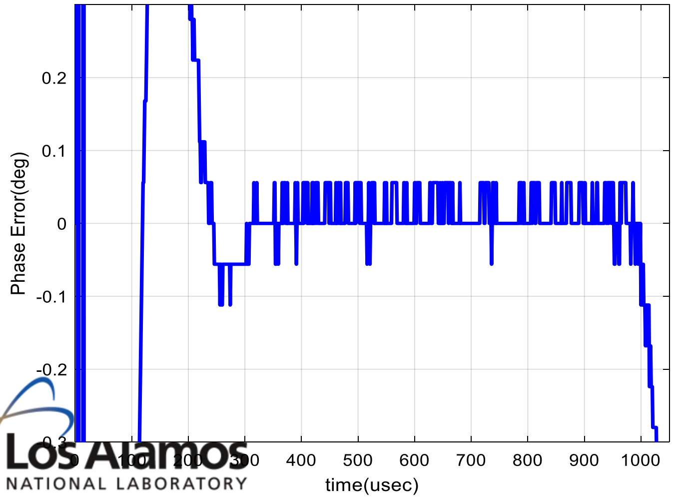
Experiments

Experiments : GUI is designed using matlab. GUI is used for interaction of the FPGA and HOST Computer. HOST Computer is a remote system plugged to the LANSCE Control Network. Both TCP/IP and UDP are supported.

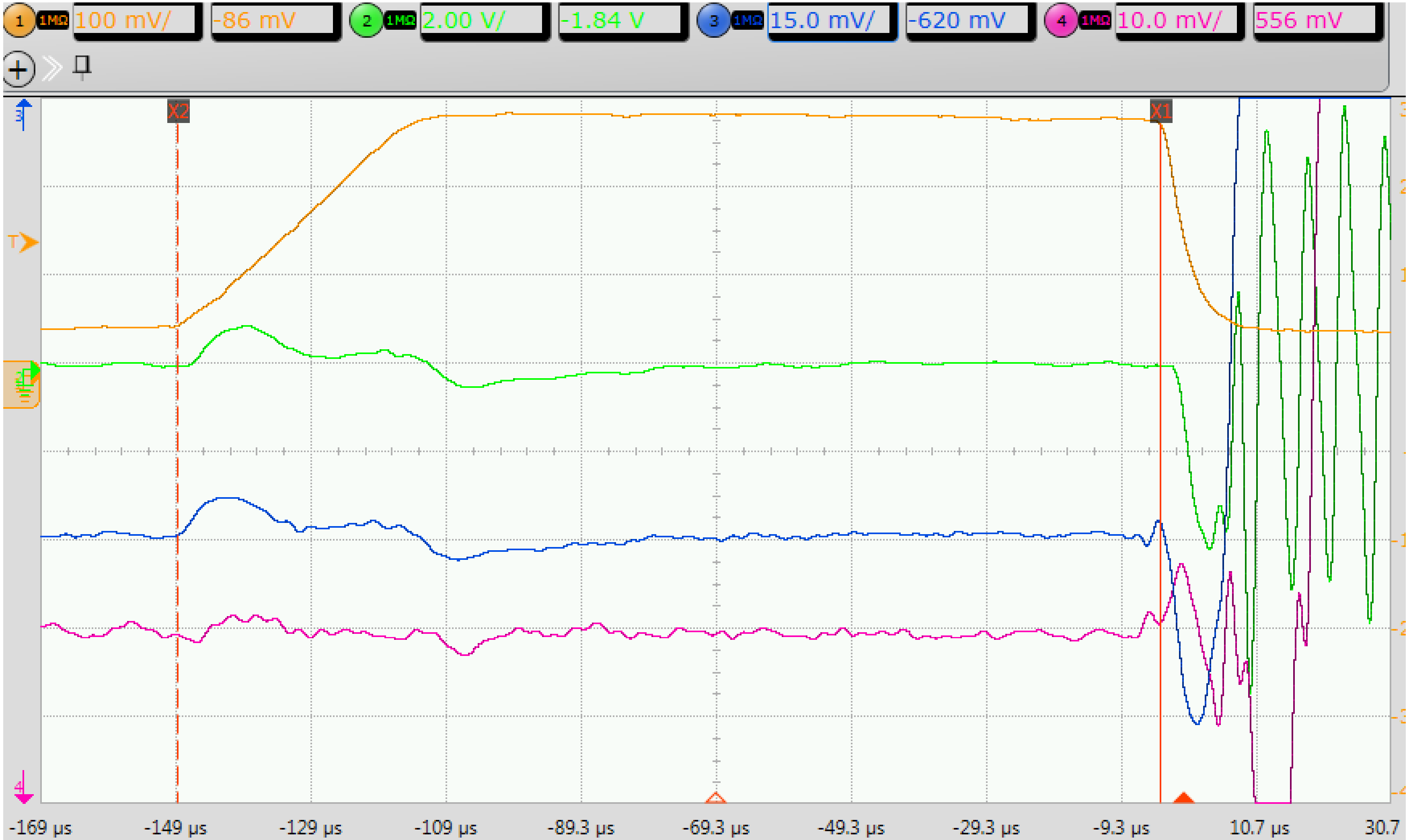
686 kW closed Loop System Test: Amplitude/Phase Response



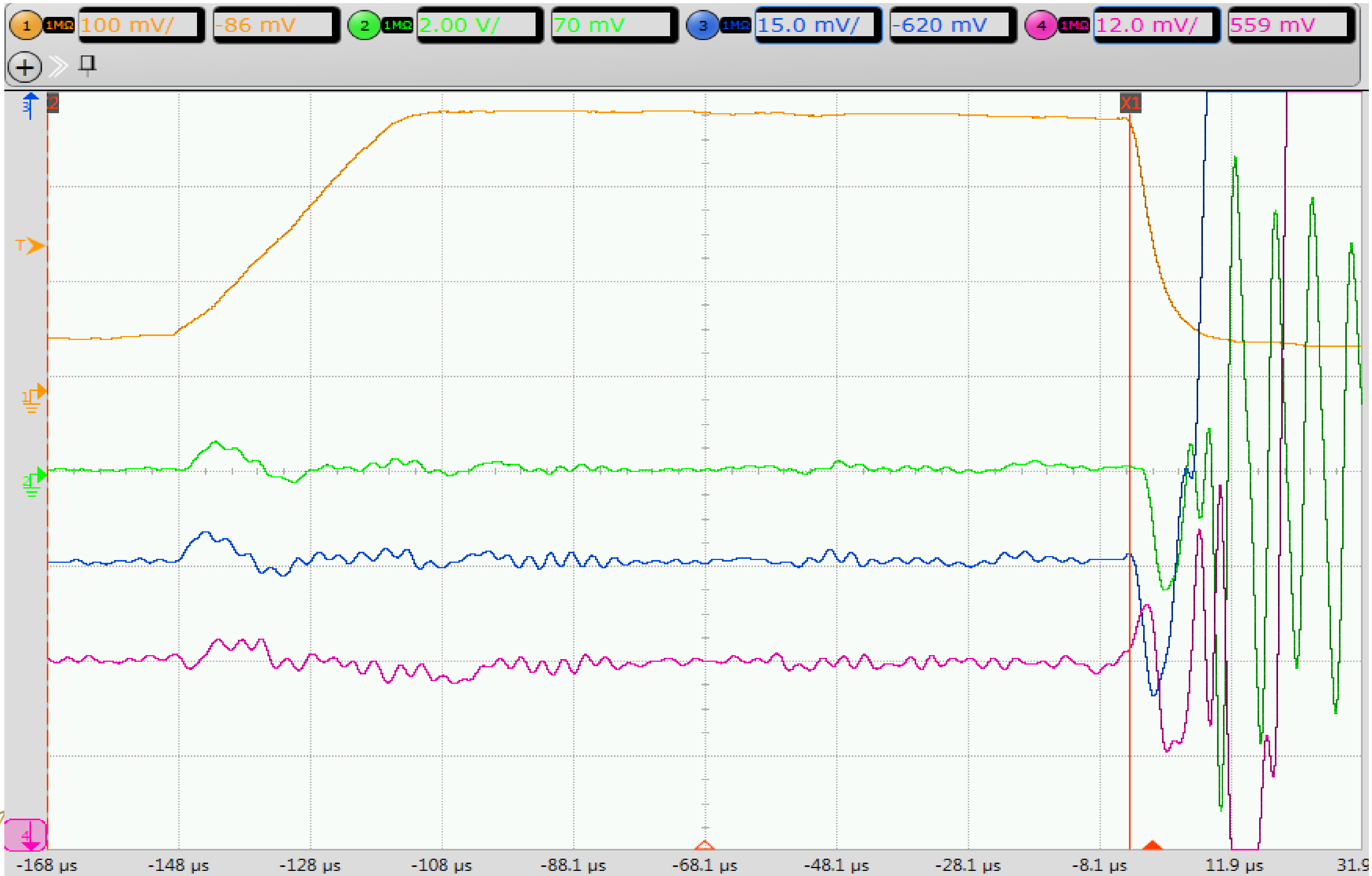




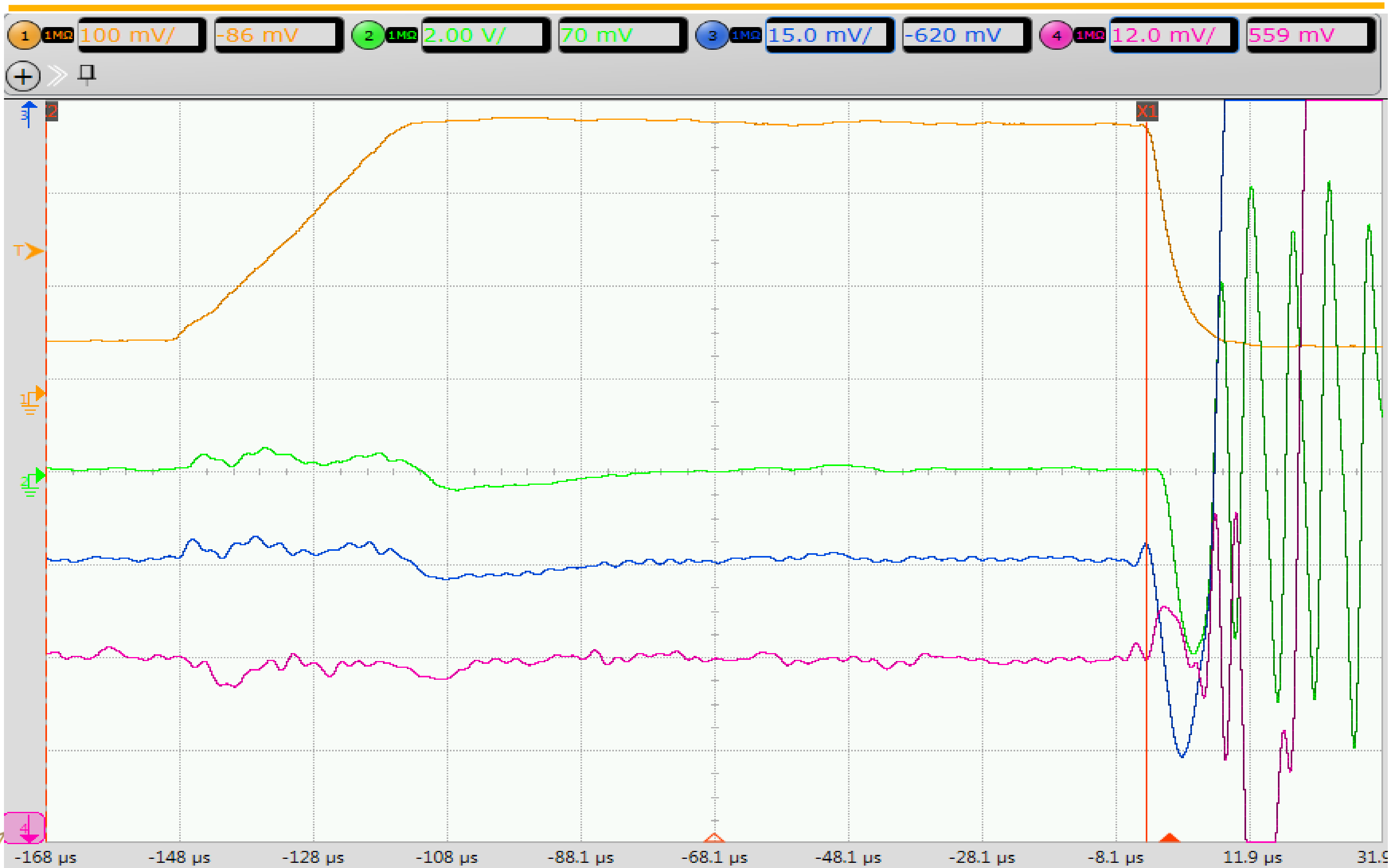
Static Beam Feedforward Controller Performance for 8mA H- Beam



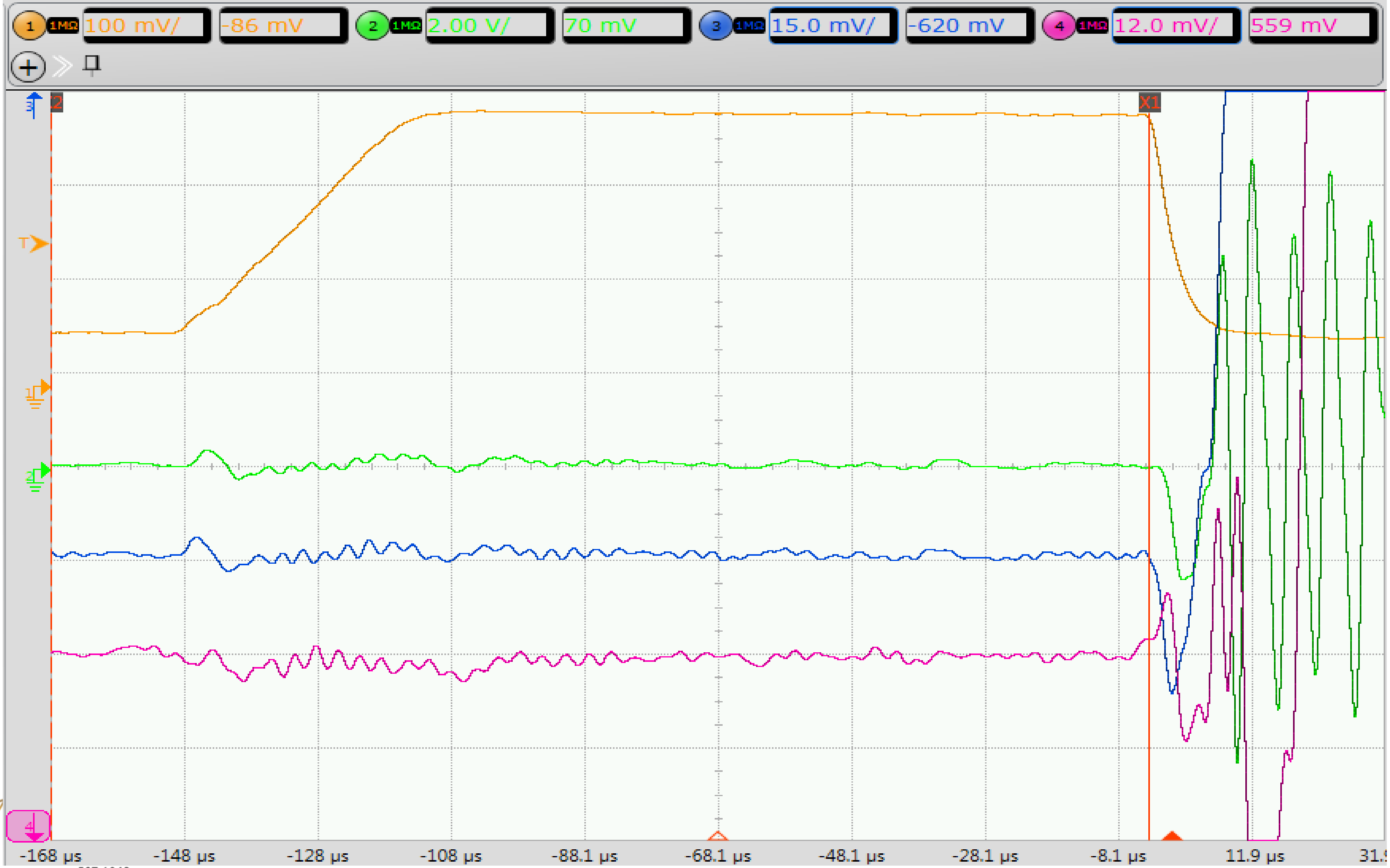
Disturbance Derivative Controller Performance for 8mA H- Beam



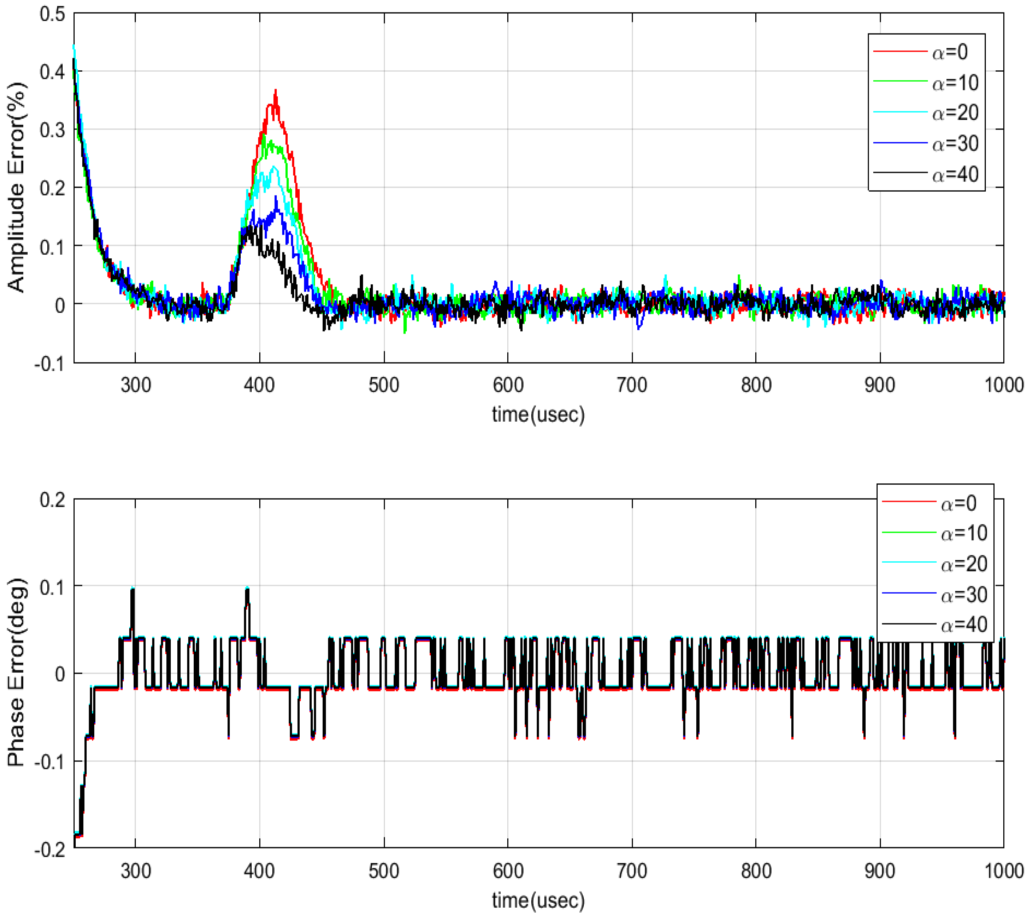
Disturbance Observer Controller Performance for 8mA H- Beam



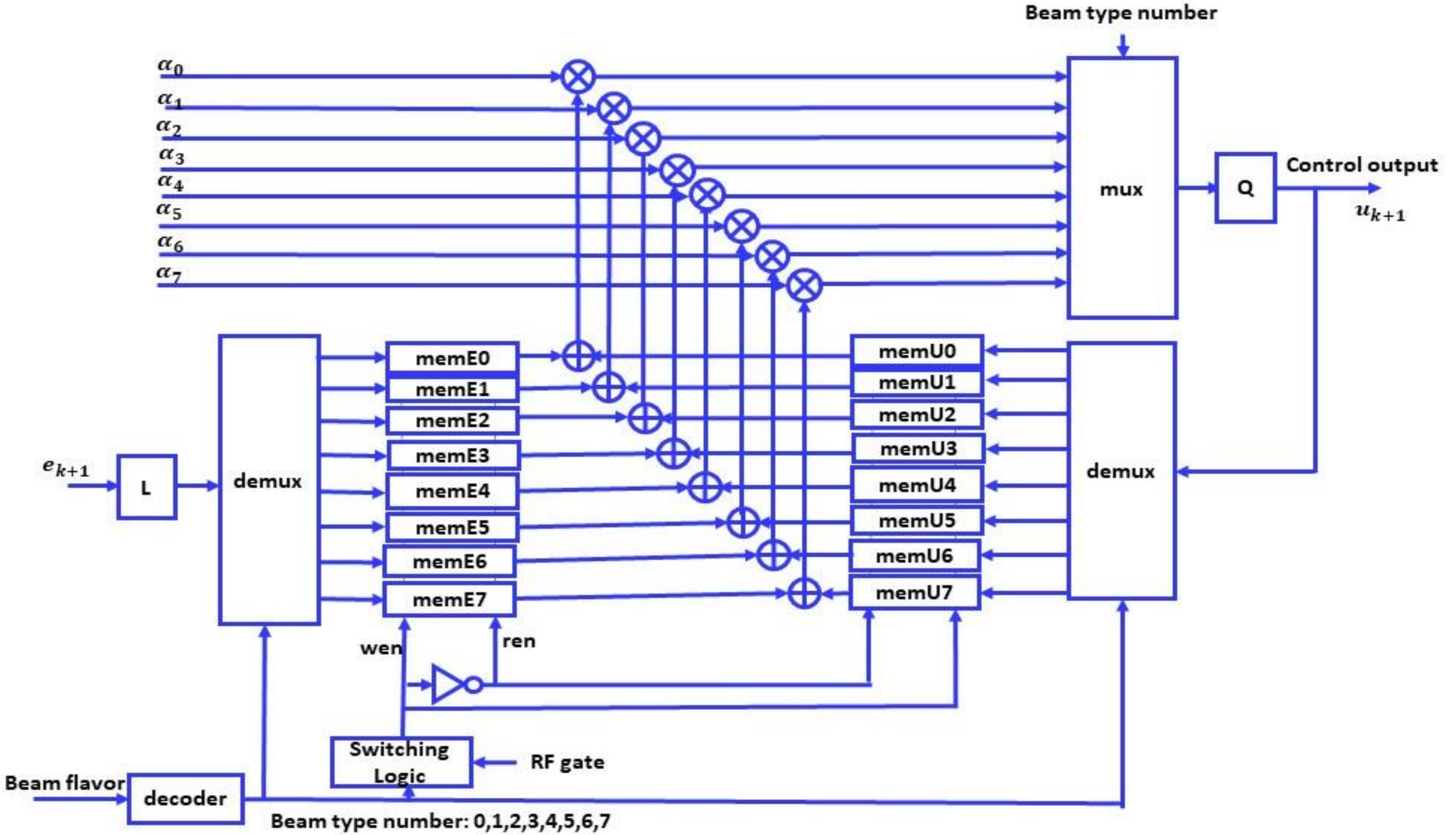
Disturbance Derivative Controller and Disturbance Observer Controller Performance for 8mA H- Beam



Iterative Learning Controller Controller Performance



Iterative Learning Controller Controller Performance



Summary

- FPGA based Digital Low Level RF System for 201 MHz DTL were developed, installed and Operated for LANSCE Beam Production
- FPGA based Digital Low Level RF System for 805 MHz SCL were developed, installed and Operated on 3 SCL for LANSCE Beam Production
- The Control System Performance Meets the design Stability of +/-1.0% and +/- 1.0 degree Specifications.
-